LOGIC SCOPE

R0214.

PM3542
PM3543

Service manual

9499 505 00211
820115

S&I

Scientific & Industrial Equipment Division

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LOGIC SCOPE

PM3542
PM3543

Service manual

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IMPORTANT

In correspondence concerning this instrument, please quote the type number and serial number as given on the type plate.

WICHTIG

Bei Schriftwechsel über dieses Gerät wird gebeten, die genaue Typenbezeichnung und die Gerätenummer anzugeben. Diese befinden sich auf dem Leistungsschild.

IMPORTANT

RECHANGE DES PIECES DETACHEES (Réparations)

Dans votre correspondance et dans vos réclamations se rapportant à cet appareil, veuillez TOUJOURS indiquer le numéro de type et le numéro de série qui sont marqués sur la plaquette de caractéristiques.

Note : The design of this instrument is subject to continuous development and improvement.
Consequently, this instrument may incorporate minor changes in detail from the information contained in this manual.

Bemerkung : Die Konstruktion und Schaltung dieses Geräts wird ständig weiterentwickelt und verbessert.
Deswegen kann dieses Gerät von den in dieser Anleitung stehenden Angaben abweichen.

Remarques : Cet appareil est l´object de dévelopments et améliorations continuels. En conséquence, certains détails mineurs peuvent différer des informations donneés dans la présente notice d´emploi et d´entretien.

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CONTENTS

		Page
1	INTRODUCTION	9
1.1.	General information	9
1.2.	Software identification code	10
1.2.1.	Documentations already published	10
1.3.	Characteristics	11
1.3.1.	Characteristics of the PM 3542	11
1.3.2.	Characteristics of the PM 3543	20
1.3.3.	Environmental characteristics for PM 3542 & PM 3543	28
1.3.4.	Mechanical data for PM 3542 & PM 3543	29
1.4.	Description of the block diagram	31
1.4.1.	State Analyzer part	31
1.4.2.	Oscilloscope part	35
2.	CIRCUIT DESCRIPTION	38
2.1.	Description of the State Analyzer part	38
2.1.1.	General Information	38
2.1.2.	Data acquisition circuit	38
2.1.2.1.	Threshold adjusting	38
2.1.2.2.	Data capturing	39
2.1.2.3.	Data acquisition memories	39
2.1.2.4.	Address counter	40
2.1.2.5.	Triggerword memories	40
2.1.2.6.	Programmable Peripheral Interface - PPI 1	40
2.1.3.	Clock and clock qualifier circuit	41
2.1.3.1.	Selection and polarity	41
2.1.3.2.	Systemclock generation	41
2.1.3.3.	Clock and data identification	42
2.1.4.	Trigger control circuit.	42
2.1.4.1.	Trigger mode circuit	42
2.1.4.2.	Generation of Clock Address Counter	46
2.1.4.3.	Generation of Clock Delay counter	47
2.1.4.4.	Delay counter	47
2.1.4.5.	TRIG OUT and TRIG IN	48
2.1.4.6.	External trigger qualifier	49
2.1.4.7.	Combi mode	49
2.1.5.	Interface oscilloscope	49
2.1.5.1.	Character generation	50
2.1.5.2.	Character position	52
2.1.5.3.	Horizontal latch	52
2.1.6.	Microprocessor, memories and decoders	53
2.1.6.1.	Microprocessor	53
2.1.6.2.	Memories	54
2.1.6.3.	Decoders	54
2.1.7.	Pushbutton interface	57
2.2	Description of the Osciloscope part	59
2.2.1.	General Information	59
2.2.2.	Vertical deflection system	59
2.2.2.1.	Input coupling	59

	Page
2.2.2.2. Input attenuator	60
2.2.2.3. Impedance converter	60
2.2.2.4. Preamplifier	60
2.2.2.5. Trigger pick off	61
2.2.2.6. Normal invert switch	61
2.2.2.7. Position control	61
2.2.2.8. Channel multivribator	62
2.2.2.9. Delay line driver	64
2.2.2.10 Composite trigger pick-off	64
2.2.2.11 Final Y-amplifier	64
2.2.3. Triggering	65
2.2.3.1. Trigger source selection	65
2.2.3.2. Trigger preamplifier	65
2.2.3.3. Impedance converter	66
2.2.3.4. Trigger comparator	66
2.2.3.5. Peak to peak level detection	66
2.2.3.6. T.V. syncronisation separator	66
2.2.4. Time base circuit	68
2.2.4.1. Time base generator	68
2.2.4.2. Sweep generator	69
2.2.4.3. Hold off circuit	70
2.2.4.4. Sweep gating logic	70
2.2.4.5. Auto sweep circuit	72
2.2.4.6. X-final amplifier	72
2.2.5. Cathode ray-tube circuit	73
2.2.5.1. CRT controls	73
2.2.5.2. Beam blanking amplifier	73
2.2.6. Power supply circuit	76
2.2.6.1. Mains transformer	76
2.2.6.2. Converter and stabilizer	76
2.2.6.3. Illumination circuit	76
2.2.7. Calibration circuit	78
3. CHECKING AND ADJUSTING	78
3.1. General information	79
3.1.1. Safety regulations	79
3.2. Test equipment and tools required	79
3.3. Power supply	80
3.3.1. Mains current	81
3.3.2. Supply section	81
3.4. Oscilloscope section	82
3.4.1. Cathode- ray tube circuit	83
3.4.1.1. Brilliance	83
3.4.1.2. Trace rotation	83
3.4.1.3. Focus and astigmatism	83
3.1.4.4. Geometry	83
3.4.2. Y-amplifier balance	84
3.4.1.1. General information	84
3.4.2.2. DC balance	84
3.4.2.3. Gain balance	84
3.4.2.4. Normal/invert balance channel B	84

Page

3.4.2.5. Shift balance 85
3.4.3. Trigger balance 85
3.4.4. Time coëfficients 86
3.4.5. Vertical amplifiers 87
3.4.5.1. General information 87
3.4.5.2. Deflection sensitivity 87
3.4.5.3. Input attenuators 88
3.4.5.4. Square-wave response final amplifier 88
3.4.5.5. Cross-talk 89
3.4.5.6. Bandwith check of channel A(B) 90
3.4.6. Triggering 90
3.4.6.1. Trigger slope 90
3.4.6.2. Trigger sensitivity 91
3.4.6.3. Trigger level internal DC 91
3.4.6.4. Trigger level auto 91
3.4.6.5. Trigger level external 91
3.4.6.6. Trigger level sensitivities 92
3.4.7. X-Deflection 93
3.4.7.1. Sensitivity 93
3.4.7.2. Frequency response 93
3.4.7.3. Horizontal sensitivity via channel A 93
3.4.7.4. Horizontal sensitivity via channel B 93
3.4.7.5. Phase difference via X and Y channels 93
3.4.8. Calibration voltage 93
3.5. Analyzer section 95
3.5.1. Intensity 95
3.5.2. Vertical size of display 95
3.5.3. Horizontal and vertical position 95
3.5.4. Threshold voltages 95
3.5.5. Systemclock SYCKP 95
3.5.6. Hold-time of data input channels 96
3.5.7. Set-up time of data input channels 96
3.5.8. Hold-time of triggerqualifier 97
3.5.9. Set-up time of triggerqualifier 97

4. INFORMATION TO ASSIST IN FAULT-FINDING 98
4.1. General information 98
4.2. Power supply 98
4.3. Trouble shooting in the oscilloscope section 98
4.4. Trouble shooting in the analyzer section 98
4.4.1. General information 98
4.4.2. Service test program 100
4.4.3. Survey of the tests 101
4.4.4. Description of the tests 101
4.4.5. Trouble shooting hints 104
4.4.5.1. Interface oscilloscope 104
4.4.5.2. Address Counter and clock circuit 104
4.4.5.3. Data Input Latches, Data Acquisition Memories 104
4.4.5.4. Trigger Control Circuit and Delay Counters 105
4.4.5.5. Information about trouble shooting equipment 105

		Page
5.	DISMANTLING THE INSTRUMENT	107
5.1.	General information	107
5.2.	Removal of instrument covers	108
5.3.	Removal of carrying handle	108
5.4.	Removal of bezel and contrast filter.	108
5.5.	Removal of control knobs and text plate	108
5.6.	Removal and replacement of the CRT and tube screen	109
5.7.	Removing the front assembly	109
5.8.	Removal of the main amplifier p.c. board	111
5.9.	Replacing switches	111
5.10.	To remove a pushbutton switch mounted on a p.c. board	111
5.11.	Removing the mains transformer	112
5.12.	Replacing the thermal fuse.	113
5.13.	Removal of power supply printed circuit board	114
5.14.	Removal of the interface printed circuit board	114
5.15.	Removal of the microprocessor printed circuit board	114
5.16.	Removal of the printed circuit boards "Options"	114
5.17.	Removal of the IC´s soldered on p.c. board	114
6.	ABBREVIATIONS AND SURVEY OF THE IC´s USED	116
6.1.	Glossary of terms and abbreviations	116
6.2.	List of IC´s used	118
6.3.	Truth tables and pin configurations of IC´s used	119
7.	PARTS LISTS (PM 3542 and PM 3543) AND DIAGRAMS (PM 3543)	145
7.1.	Mechanical parts	145
7.2.	Electrical parts	148
7.3.	Miscellaneous parts	165
8.	PM 3542 INFORMATION	181
8.1.	General information	181
8.2.	Hardware differences	181

LIST OF ILLUSTRATIONS

Figure	Title	Page
1.1.	Logic scope, model PM 3543	9
1.2.	Minimal signal swing	12
1.3.	Definition of the set-up an hold times	12
1.4.	Dimensions of the cabinet	29
1.5.	Block diagram of the State Analyzer part	32
1.6.	Block diagram of the Oscilloscope part	36
2.1.	Tabel of triggermode selector signals	43
2.2.	Generation of the signal Clock Address counter	46
2.3.	Generation of the signal Clock Delay counter	47
2.4.	Character presentation	50
2.5.	Memory map	55
2.6.	Pushbutton matrix	58
2.7.	Vertical deflection system	59
2.8.	Simplified diagram of the channel multivibration	62
2.9.	Trigger circuit	65
2.10.	Signal on the base of transistor V1015	67
2.11.	A vertical interval with frame synchronisation pulse group	67
2.12.	Time-base generator	68
2.13.	Sweep gating logic signals	70
2.14.	Time relation diagram of the sweep gating logic in the AC or DC mode	71
2.15.	Cathode-ray tube circuitry	73
2.16.	Shunt feed-back amplifier	74
2.17.	Power supply	76
2.18.	Basic diagram of the converter	77
3.1.	Adjusting and checking of the power supply	82
3.2.	Adjusting elements attenuator board	86
3.3.	Adjusting elements amplifier board	94
4.1.	Flow chart of the sequence of service self tests	99
4.2.	Front view of the jumper connection	100
4.3.	Use of logic pulser and indicator probes	105
5.1.	Removing the instrument covers	107
5.2.	Removing the bezel and the contrast plate	108
5.3.	Removal of the amplifier board	110
5.4.	Removal of the attenuator board	110
5.5.	Replacing a switch segment	111
5.6.	Push button set clamping device	112
5.7.	Removing the mains transformer	113
5.8.	Replacing the thermal fuse	113

Figure	Title	Page
6.0.	Truth tables and pin configuration of IC´s used	119
7.1.	Front view showing item numbers	145
7.2.	Side view showing item numbers	146
7.3.	A.C. compartment showing item numbers	147
7.4.	L.S. Analyzer p.c. board	170
7.5.	Data Acquisition circuit	171
7.6.	Clock, Qualifier and Triggercontrol circuit	173
7.7.	Microprocessor system	175
7.8.	Interface oscilloscope board	176
7.9.	Interface oscilloscope circuit	177
7.10.	Vertical attenuator p.c. board	180
7.11.	Power supply p.c. board	180
7.12.	Amplifier p.c. board	180
7.13.	Circuit diagram of the complete oscilloscope part	181
8.1.	Data aquisition circuit PM 3542	185
8.2.	Block diagram of the State Analyzer part PM 3542	186

1. INTRODUCTION

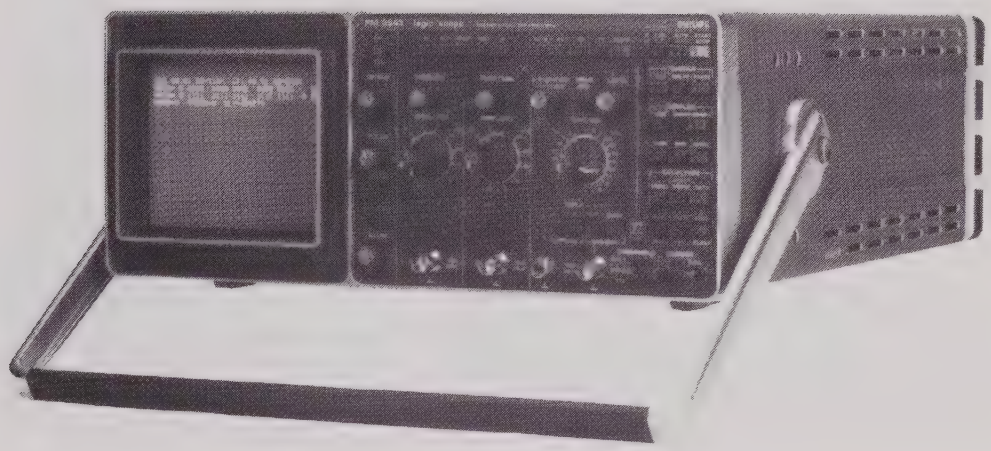


Fig. 1.1. Logic scope, model PM 3543

1.1. General information

This manual contains all the information necessary to service the Logic Scopes PM 3542 & PM 3543.
Characteristics, circuit diagrams and spare parts lists indicate the differences between the PM 3542 and PM 3543.
The Chapters : Circuit description, Checking and adjusting, Information to assist in fault finding and Dismantling the instrument is based on the PM 3543. The information in these chapters is also valid for the PM 3542 and occuring differences are mentioned.

1.2. Software identification code

The Software identification code identifies the release version of the software package and the status of the built in options of the Logic Scope.
This code appears on the screen if the service test program is selected (i.e. by depressing the START/STOP, DECR/0 and the ROLL up keys simultaneously). See also chapter 4.4.2.

Example: 4302 - S02 - DA01

43 : type number Logic Scope
02 : release version of main program
S : RS232C serial interface is built-in
(P : character P is displayed incase an IEC 625 interface is built-in)
02 : release version of serial interface software
DA : disassembler package A
01 : release version of disassembler package.

1.2.1. Documentations already published

Type	Language	Ordering number
Operating manual PM 3542	(English)	9499 500 10511
Operating manual PM 3543	(English/French/German)	9499 500 10801
Options manual PM 3542/PM 3543	(English)	9499 500 10711
Reference card PM 3542 & PM 3543	(English)	9499 500 10911

1.3.Characteristics

This instrument has been designed and tested according to IEC Publication 348 for Class II instruments and has been supplied in a safe condition.
The present Manual contains information and warnings which shall be followed by the purchaser to ensure safe operation and to maintain the instrument in a safe condition.

Properties expressed in numerical values with state tolerances are guaranteed for ambient temperature of +5 degC ... +40 degC unless stated otherwise. Numerical values without tolerances are worst-case and represent the characteristics of an average instrument. This specification is valid only after the instrument has warmed up for 15 minutes.

OPERATION MODES
- Logic State Analyzer mode
- Oscilloscope mode
- Combi mode : analyzer triggers oscilloscope

1.3.1. Characteristics of the PM 3542

Characteristics of the analyzer part

Analyzer inputs : - 2 multi-lead input sockets at rear-side providing:
- 11 ... 13 data channels
- 2 clocks
- 1 ... 3 clock qualifiers

} via 2 connectors

Data input
All values are worst-case values and specified at the probe tip(s)
: By clock states or triggers via 2 probe pod's PM 8821 providing connections for 8 inputs each :
- probe 1 : data channels 0 ... 7
- probe 2 : data channels 8 ... 10/12
  clock CK0 + CK1
  clock qualifiers Q1, Q2, Q3

Impedance : 4 MΩ //6 pF

Max. Voltage : - 50V ... + 50V

Threshold : TTL, 1,4 V fixed
VAR1, Variable -3 ... 12 V contineously adjustable.
VAR2, Variable -3 ... 12 V continuously adjustable.

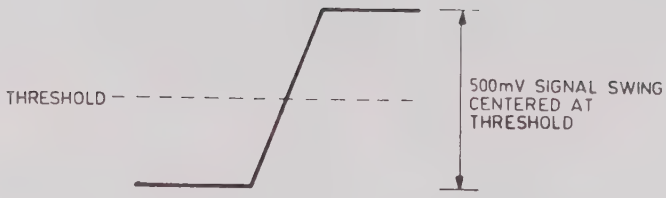


Fig. 1.2. Minimal signal swing

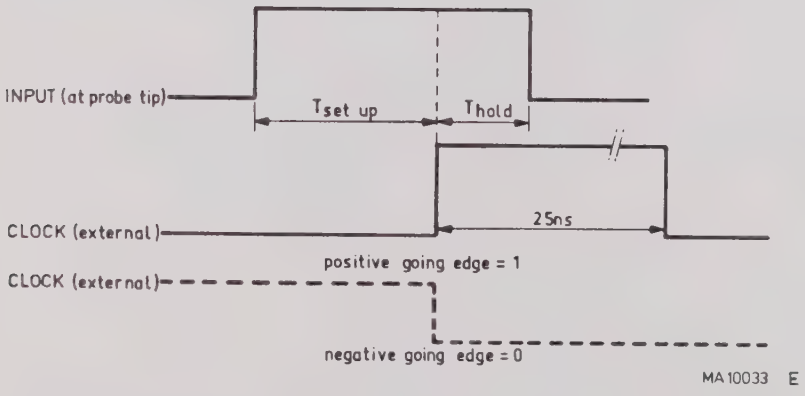


Fig. 1.3. Definition of set-up and hold times

Max. Sensitivity : 0,5 V p-p signal swing (see Fig. 1.2.).

Set-up and hold-time : Set up time = 35 nsec (see Fig. 1.3.)
Hold-time = 0
with respect to probe-tip

Clocks : 2, main clock, CK0, must always be connected.

Clock input : via logic pod PM 8821. Max input voltage + 50 V

Source : System under test

Threshold : Same specifications as data input

Repetition time (min.) : 100 nsec.

Clock pulse width (min.): 25 nsec. (see Fig. 1.3.)

Sampling : Selectable on positive or negative going clock edges

Clock qualifiers : 3 clock qualifiers for each clock. Input via probe pod PM 8821. These clock qualifiers are interchangeable fixed

Threshold : Same specification as data input

Sampling : Only occurs when qualifiers "true" at selected active clock edge.

"True" selection : "1" for high
"0" for low
"X" for don´t care (qualifier not in use)

Set-up and hold-time : Set up time = 25 nsec
Hold-time = 0 nsec
with respect to probe tip (see Fig. 1.3.)

Triggering : Three trigger modes can be selected in menu-mode under control of the execute switches.
- parallel : clock CK0 is selected. Triggering if the triggerword is recognized.
- quasi-parallel : two clocks selected. Triggering if immediately after the first trigger word is recognized, at CK0, the second is found, at CK1.
- sequential : pushbutton SEQ, trigger selection, depressed.
  Triggering is after the first trigger word, at CK0, the second, at selected CK0 or CK1, is recognized.

Trigger delay : Max. trigger delay 65535 clock states (s) or triggers (T) controlled in menu mode by execute switches. On the screen is displayed when and where a delay is selected (D).

Trigger word selection : - bit by bit in menu mode under control of cursor and execute pushbuttons.
- complete word out of the data stream under control of pushbuttons TRIGW and EXCH/X.

Trigger qualifier : Input via front panel BNC socket, TRIG QUAL, selected by depressing EXT and WORD simultaneously.
Level can be selected in menu mode by the execute switches.

TRIG IN : BNC socket at the rear-side of the instrument for trigger probe PM 8810. "1" = true, TTL level.

TRIG OUT : BNC socket at the rear side of the instrument of trigger probe PM 8810 "1" = true, TTL level.

False triggering : Controlled via pushbutton FALSE. When depressed triggering if captured data doesn´t match the trigger word.

Start/Stop

Source : Automatic or manual

Automatic : Automatic start of data capturing after a display time of approximately 1 second.

Manual : Data acquisition has to be started by pressing START/stop.

Stop : Data acquisition can be stopped manual by pressing start/STOP.

Memory : The memory format is 255 x 16 bits
255 x 13 bits are used for data storage.
In compare mode a second memory of the same size is used.

Display : Cathode ray-tube of oscilloscope.

Heading : Top part of the screen continuously displayed, giving the parameters and status of the instrument.

Display window : 12 samples of data displayed at the same time on the screen can be shifted through the memory by the ROLL tumbler switch.

Line-numbering : Trigger word (in quasi-parallel and sequential triggermode, the second) is indicated as TRIG. The line-numbers are related to the triggerword position.

Cursor : In menu mode horizontally and vertically positionable intensified character.

Data handlings : Data can be blanked, recalled and inverted under control of cursor " ^ " which is horizontally positionable.

Display modes :
- Parallel : only clock CK0 selected. Pod numbers above the data columns and clock number behind each data sample.
- Parallel : two clocks selected, CK0 and CK1. Pod and clock numbers above the data columns. Two data samples as one line.
- Sequantial mode : one or two clocks selected. Pod number above the data columns and clock number behind every data sample. One data sample on one line.

Data formats : In both display modes, parallel and sequential data is displayed on the screen in hexadecimal and binary format at the same time.

Compare : Contents of Data Acquisition Memory is compared with the contents of the Reference Memory, which is loaded under control of pushbutton DATA and the execute pushbuttons. Depending the result of the comparison "EQ" or "NEQ" is displayed.

Characteristics of the oscilloscope part

Including the combined analyzer/oscilloscope functions with the trigger sources
- A, B, Composite and EXT
- WORD, via Analyzer

Designation	Specification	Additional Information
C.R.T.		
Type	D14 - 125 GH/08	
Measuring data	8x10 divisions	1 div. equals 1 cm
Screen type	P31 (GH)	P7 (GM) optional
Total acceleration voltage	10 kV	
Graticule	Internal	Cont. variable illumination
Vertical amplifier		
Display mode	Channel A only Channel B only A and B chopped A and B alternated A and B added	
Channel B polarity	Normal or inverted	
Response :		
Frequency range	DC: 0 Hz ... 35 MHz (-3 dB) AC: 2 Hz ... 35 MHz (-3 dB)	
Rise time	$\leqslant$ 10 ns	
Pulse aberrations	$\leqslant$ +/- 3% ($\ll$ 4% pp)	Measured at 6 div. amplitude and applied time of > 1 ns
Deflection coefficients	2 mV/DIV... 10V/DIV	1-2-5 sequence
Continuous control range	1 : $\geqslant$ 2,5	
Deflection accuracy	+/_ 3%	
Input impedance	1 MΩ //20 pF	
Input RC time	0,1 s	Coupling switch to AC

Maximum permissible input voltage	400V, d.c. + a.c. peak	
Chopping frequency	about 500 kHz	
Vertical positioning range	16 divisions	
Dynamic range	24 divisions	
Visible signal delay	$\geqslant$ 2 divisions	At 10 ns
C.M.R.F. in A-B mode	$\geqslant$ 40 dB at 1 MHz	After adjustment at d.c. or low frequencies
Cross talk between channels	-40 dB or better at 10 MHz	Both attenuators in the setting
Instability of the spot position:		
Temperature drift	$\leqslant$ 0,3 div./hour	

Time base

Time coefficients	0.5 s/DIV ... 0.2 us/DIV	1-2-5 sequence
Continuous control range	1 : $\geqslant$ 2.5	
Coefficient error	+/_ 3%	
Magnification	10 x	
Magnifier error	+/_ 2%	

Triggering

Source	External	Via front panel BNC socket, TRIG QUAL
	Internal	- via oscilloscope, A,B or Composite - via analyzer: at selected trigger conditions WORD depressed.

Triggermode	Automatic, normal AC normal DC and TV	TV line or frame switched by TV line : 1µs/div...20µs/div TV frame : 50µs/div...5s/div
Trigger sensitivity	Internal:1.0 DIV at 35 MHz External:0.2 Vpp at 35 MHz TV int.: 0.7 DIV TV ext.: 0.15 Vpp	 Sync pulse amplitude Sync pulse amplitude
Triggering frequency range	AUTO: 20 Hz... $\geqslant$ 35 MHz AC : 5 Hz ... $\geqslant$ 35 MHz DC : 0 Hz ... $\geqslant$ 35 MHz	Typically, stable triggering can still be obtained at 50 MHz and 2 div. or 1 Vpp amplitude
Level range	AUTO : Proportional to peak-to-peak value of trigger signal. AC, DC: 16 div. at Internal trigg. 3,2 V at external trigg.	 + or - 8 div. and + or - 1,6 V reference to centre of screen.
Triggering slope	Positive or negative going	
Input impedance	1 MΩ //20 pF	
Maximum permissible input voltage	400 V, d.c. + a.c. peak	below 100 kHz
Hold-off time	variable	
X Deflection		
Source	A, B, EXT	As selected by trigger source switch, if TIME/DIV switch is in pos. TRIG or X DEFL.
Deflection cooefficients	A or B: As selected by AMPL/DIV EXTERNAL : 0.2 V/DIV	
Deflection accuracy	+/_ 10%	
Frequency range	DC : 0 Hz ... 1 MHz (-3 dB) AC : 5 Hz ... 1 MHz (-3 dB)	

Phase shift	⩽ 3 deg at 100 kHz	
Dynamic range	24 divisions	For frequencies ⩽100 kHz

Calibration generator

Output voltage	1.2 Vpp	Square wave
Accuracy	+/_ 1%	
Frequency	about 2 kHz	

Power supply

AC supply :	Double insulated	Safety Class II, IEC348
Nominal voltage range (on line mains voltage adaptor)	110,127,220 or 240 Vac +/_ 10%	
Nominal frequency range	50Hz .. 400 Hz +/_ 10%	
Power consumption	59 W 63 W	At nominal mains voltage with options
DC supply :		
Voltage range	24,5 - 27 V	
Current consumption	1,6 A 1,7 A	 With options
Capacity to earth	110 pF 23 pF	Measured with rubber feet on earthed metal plate of 1 m2. Measured 30 cm above earthed plate of 1 m2

1.3.2. Characteristics of the PM 3543

Characteristics of the analyzer part

Analyzer inputs	: 3 multi-lead input sockets at rear-side providing: - 19 ... 21 data channels - 2 clocks - 1 ... 3 clock qualifiers
Data input and specified at the probe tip(s) (All values are worst-case values)	: By clock states or triggers via 3 probe pod´s PM 8821 providing connections for 8 inputs each : - pod 0 : data channels 0 ... 7 - pod 1 : data channels 8 ... 15 - pod 2 : data channels 16 ... 18/20 other inputs used for clocks and clock qualfiers
Impedance	: 4 MΩ // 6 pF
Max. Voltage	: - 50 V ... + 50 V
Threshold	: TTL, 1,4 V fixed. VAR1, Variable -3 ... 12V continuously adjustable. VAR2, Variable -3 ... 12V continuously adjustable.
Max. Sensitivity	: 0,5 V p-p signal swing (see Fig. 1.2.).
Set-up and hold-time	: Set up time = 35 nsec (see Fig. 1.3.) Hold time = 0 with respect to probe-tip
Clocks	: 2, main clock, CK0, must always be connected.
Clock input	: via pod 2 (Logic pod PM 8821). Max. input voltage +/_ 50 V
Source	: System under test
Threshold	: Same specification as data input
Repetition time (min.)	: 100 nsec.
Clock pulse width	: 25 nsec (see Fig. 1.3.)
Sampling	: Selectable in positive or negative going clock edges

Clock qualifiers : 3 clock qualifiers for each clock.
These clock-qualifiers are interchangeable fixed.

Clock qualifier input : via pod 2 (Logic pod PM 8821). Max. input voltage +/_ 50 V.

Threshold : Same specification as data input

Sampling : Only occurs when qualifiers "true" at selected active clock edge.

"True" selection : "1" for high
"0" for low
"X" for don´t care (qualifier not in use)

Set-up and hold-time : Set up time = 25 nsec
Hold-time = 0 nsec
with respect to probe tip (see Fig. 1.3.)

Triggering

Trigger modes : Four trigger modes can be selected.
- parallel : one triggerword, with CK0, selected. Triggering if the triggerword is recognized.
- quasi-parallel : two triggerwords and two clocks CK0 and CK1 selected. Triggering if immediately after the first triggerword, on CK0, the second, on CK1, is recognized.
- sequential : pushbutton SEQ, TRIGGER section, depressed.Two triggerwords and one or two clocks selected. Triggering if after the first trigger-word, on CK0, the second, on selected clock, is recognized.
- immediate sequential : pushbutton SEQ, TRIGGER section, depressed Triggering if immediately after the first trigger-word with CK0 the second is founded with CK0.

Trigger delay : Max. trigger delay 65536 clock states (S) or triggers controlled in menu mode by execute switches. The position and value of the trigger delay are displayed in the heading.

Trigger word selection : - bit by bit in menu mode under control of cursor and EXECUTE pushbuttons.
- complete word out of the data stream under control of pushbuttons TRIGW and EXCH/X.

Trigger qualifiers : Input by passive probe PM 8927 via front panel BNC socket, TRIG QUAL.
Selected by depressing EXT and WORD simultaneously. Hold and set-up time as clock qualifiers. Level and position can be selected in menu mode by the EXECUTE switches.

TRIG IN : BNC socket at the rear-side of the instrument for trigger probe PM 8810.
"1" = true, TTL level. Max. input voltage +/_ 50 V
Set-up time : min. 0 ns. Hold time : max. 50 ns.

TRIG OUT : BNC socket at the rear side of the instrument for triggering other equipment "1" = true , TTL level.

False triggering : Controlled via pushbutton FALSE. When depressed triggering if captured data doesn't match the second trigger word.

Start/Stop

Source : Automatic or manual

Manual : Data acquisition has to be started by pressing START/stop.

Automatic : After START is pressed data capturing is automatically repeated after a display time of approximately 1 second.

Stop : Data acquisition can be stopped manual by pressing start/STOP.

Memory : The memory format is 256 x 24 bits
255 x 21 bit are used for data storage.
In compare mode a second memory of the same size is used.

Display : Cathode ray-tube of oscilloscope.

Heading : Top part of the screen continuously displayed, giving the parameters and status of the instrument.

Display window : 12 data words displayed on the screen. The window can be shifted through the memory by the ROLL tumbler switch.

Line-numbering : The line-numbering are related to the position of the (second) triggerword.

Cursor : - In menu mode horizonally and vertically positionable flashing intensified character in the heading.
- Horizontally positionable " Λ " sign above displayed data columns.

Data handlings : Data can be blanked, recalled and inverted under control of cursor " Λ " which is horizontally positionable.

Display modes : _ parallel : pod and clock numbers above data columns.
_ sequential : pod numbers above data columns and clock numbers behind each data sample, so one data sample per line.
If one clock (CK0) is selected data is always displayed sequential. If two clocks are selected data can be displayed parallel or sequential by manipulating pushbutton SEQ, DISPLAY section.

Data formats : Data can be displayed in hexadecimal and binary format. In parallel display mode only two data columns can be displayed binary. These columns can be selected under control of cursus " Λ " and EXCH, in display section.

Graph : The displayed dots on the screen represent a 16 bit word, which value can be read on the vertical axis and the sequence of capturing these words is represented by the horizontal axis.

Compare : Contents of Data Acquisition Memory is compared with the contents of the Reference Memory, which is loaded under control of pushbutton DATA and the EXECUTE pushbuttons. Depending the result of the comparison "EQ" or "NEQ" is displayed.

Characteristics of the oscilloscope part

Including the combined analyzer/oscilloscope functions with the trigger sources.
- A, B, COMPOSITE and EXT
- WORD, via Analyzer

Designation	Specification	Additional Information
C.R.T.	D14-125 GH/08	
Measuring data	8 x 10 divisions	1 div. equals 1 cm
Screen type	P31 (GH)	P7 (GM) optional
Total acceleration voltage	10 kV	
Graticule	Internal	Cont. variable illumiation
Vertical amplifier		
Display mode	Channel A only Channel B only A and B chopped A and B altenated A and B added	
Channel B polarity	Normal or inverted	
Response :		
Frequency range	DC : 0 Hz ... 35 MHz (-3 dB) AC : 2 Hz ... 35 MHz (-3 dB)	
Rise time	$\leqslant$ 10 ns	
Pulse aberrations	$\leqslant$ +/_ 3% ($\leqslant$ 4 % pp)	Measured at 6 div. amplitude and applied rise time of $\geqslant$ 1 ns
Deflection coefficients	2 mV/DIV ... 10 V/DIV	1-2-5 sequence
Continuous control range	1 : $\geqslant$ 2,5	
Deflection accuracy	+/_ 3 %	

Input impedance	1 MΩ // 20 pF	
Input RC time	0.1 s	Coupling switch to AC
Maximum permissible input voltage	400 V, d.c. + a.c. peak	
Chopping frequency	about 500 kHz	
Vertical positioning range	16 divisions	
Dynamic range	24 divisions	
Visible signal delay	⩾ 12 divisions	At 10 ns
C.M.R.F. in A-B mode	⩾ 40 dB at 1 MHz	After adjustment at d.c. or low frequencies
Cross talk between channels	- 40 dB or better at 10 MHz	Both attenuators in the same setting
Instability of the spot position:		
Temperature drift	< 0,3 div/hour	

Time base

Time coefficients	0.5 s/DIV ... 0.2 us/DIV	1-2-5 sequence
Continuous control range	1 : ⩾ 2,5	
Coefficient error	+/_ 3%	
Magnification	10 x	
Magnifier error	+/_ 2%	

Triggering

Source	External	Via front panel BNC socket, TRIG QUAL.
	Internal	- via oscilloscope; A,B or Composite - via analyzer; at selected trigger conditions and WORD depressed.

Triggermode	Automatic, normal AC, normal DC and TV	TV line or frame switched by TIME/DIV switch TV line: 1 µs/div...20 µs/div. TV frame: 50 µs/div...5 s/div.
Trigger sensitivity	Internal : 1.0 DIV at 35 MHz External : 0.2 Vpp at 35 MHz TV int.: 0.7 DIV TV ext.: 0.15 Vpp	 Sync pulse amplitude Sync pulse amplitude
Triggering frequency range	AUTO: 20 Hz ⩾ 35 MHz AC : 50 Hz ⩾ 35 MHz DC : 0 Hz ⩾ 35 MHz	Typically,stable triggering can still be obtained at 50 MHz and 2 div. or 1Vpp amplitude
Level range	AUTO : Proportional to peak-to-peak value of trigger signal. AC, DC: 16div. at internal trigg. 3,2V at external trigg.	 + or - 8 div. and + or _ 1,6V reference to centre of the screen
Triggering	Positive or negative going	
Input impedance	1 MΩ//20 pF	
Maximum permissible input voltage	400 V, d.c. + a.c. peak	below 100 kHz
Hold-off time	variable	
X-deflection		
Source	A, B, EXT	As selected by trigger source switch, if TIME/DIV switch is in pos. TRIG or X DEFL
Deflection coefficient	A or B : As selected by AMPL/DIV EXTERNAL : 0.2 V/DIV	
Deflection accuracy	+/_ 10 %	

Frequency range	DC:0 Hz...1 MHz (-3 dB) AC:5 Hz...1 MHz (-3 dB)	
Phase shift	⩽ 7 degC at 100 kHz	
Dynamic range	24 divisions	For frequencies ⩽100 kHz

Calibration generator

output voltage	1.2 Vpp	Square wave
Accuracy	+/_ 1 %	
Frequency	about 2 kHz	

Power supply

AC supply:	Double insulated	Safety Class II, IEC 348
Nominal voltage range (on line-mains voltage adaptor)	110,127,220 or 240 Vac +/_ 10 %	
Nominal frequency range	50 ... 400 Hz +/_ 10 %	
Power consumption	60 W 64 W	At nominal mains voltage with options
DC supply :		
Voltage range	24,5 - 27 V	
Current consumption	1,7 A 1,8 A	With options
Capacity to earth	110 pF	Measured with rubber feet on earthed metal plate of 1 m2
	23 pF	Measured 30 cm above earthed plate of 1 m2
Note :	Battery pack PM 8901 can not be used.	

1.3.3. Environmental characteristics for PM 3542 & PM 3543

The environmental data are valid only if the instrument is checked in accordance with the official checking procedure. Details on these procedures and failure criteria are supplied on request by the PHILIPS organisation in your country, or by N.V. PHILIPS' GLOEILAMPENFABRIEKEN, TEST AND MEASURING DEPARTMENT, EINDHOVEN, THE NETHERLANDS.

Ambient temperatures :

Rated range of use	+ 5 degC ... + 40 degC
Operating	- 10 degC ... + 45 degC
Storage and transpot	- 40 degC ... + 70 degC

Altitude :

Operating to	5000 m (15000 ft)
Non-operating to	15000 m (45000 ft)

Relative humidity	Rated range of use.	20%...80%	No condensation
	Limited range for storage and transport.	5%...95%	
	Recovery time.	30 min.	If the instruments temperature is raised from -10degC to +20 degC at 60% relative.

Shock	30 g : half sinewave shock of 11 ms duration : 3 shock per direction for a total of 18 shocks

Vibration	Rated range of use	Negligible value	
	Limited range for storage and transport	0,7 mm/pp max. 50m/s2	Frequency range 10...150 Hz
Bump	Rated range of use	10 m/s2 6 ms	
	Limited range for storage and transport	100 m/s2	1000 times, 6 ms in each 3 directions

Electromagnetic interference	Meets VDE 0871 and VDE 0875 level B.
Safety	The isolation between the instruments and line fulfils the safety requirements of IEC 348 for metal encased class II instruments.

1.3.4. Mechanical data for PM 3542 & PM 3543

Dimensions	See Fig. 1.4.	
Length	445 mm	Hardle and controls excluded
Width	335 mm	Handle excluded
Height	137 mm	Feet excluded
Weight	9,8 kg	

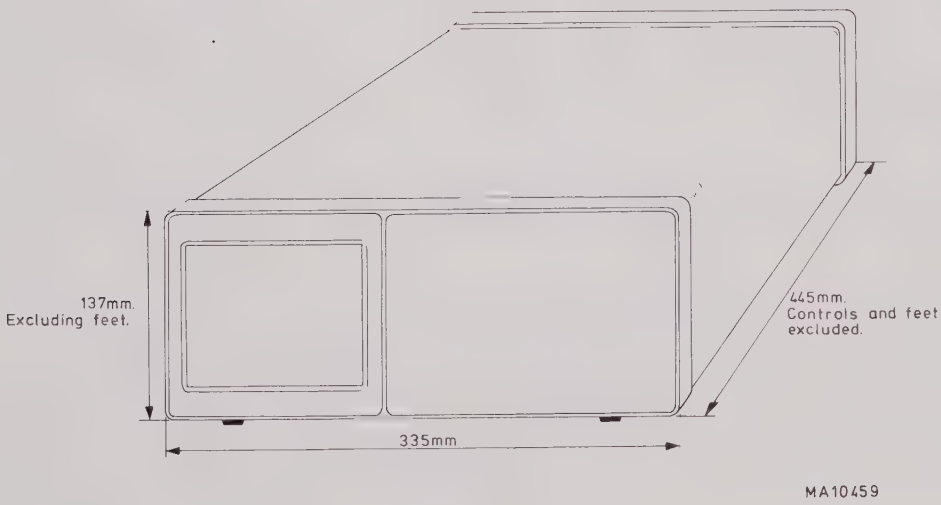


Fig. 1.4. Dimensions of the cabinet

1.3.5. Accessories

1.3.5.1. Supplied with the instrument

Front-cover
1 BNC 4 mm adaptor
3 oscilloscope probe´s PM 8927
User manual
3 multi-lead pods PM 8821. For PM 3542 only 2 multi-lead pods are delivered.

1.3.5.2. Optional

The following options can be ordered and installed in the logic-scope :

- PM 8843/20 : RS232C serial and audio cassette interface
- PM 8843/40 : IEC 625 parallel interface
- PM 8843/60 : RS232C serial and audio cassette and disassembly package
- PM 8843/80 : IEC 625 parallel interface and disassembly package

For the PM 3542 these typenumbers are :
- PM 8842/20, PM 8842/40, PM 8842/60 and PM 8842/80.

These optionals are factory fitted in the Logic Scope versions,
PM 3543/20, /40, /60 and /80.

Oscilloscopes probes :

Passive probe 1 : 1	PM 8921 (L)
Passive probe 10 : 1	PM 8925 (L)
Passive probe 100 : 1	PM 8932
Active probe	PM 8940
Fet probe	PM 8943
Current probe	PM 9355/01

Analyzer probes :

Multi-lead probe	PM 8821
Extension kit	PM 8819
Logic trigger probe	PM 8810

Sundries :

Oscilloscope camera	PM 9381
Adapter for PM 9381	PM 8972
Polaroid filter	PM 8910
Viewing hood´s	PM 9366, PM 8980
19-in rackmount	PM 8963

1.4.Description of the block diagram (see Figure 1.5.)

1.4.1. State analyzer part

Microprocessor system
The operations of the state-analyzer are controlled by an 8085A microprocessor (uP).
The 8085 has an 8-bit data bus and a 16-bit address bus. The eight least significant bits of the address bus are time-multiplexed with the data bus. This address-data bus is demultiplexed by the Address Latch (D2338) under control of the microprocessor´s ALE signal.
The program, executed by the microprocessor, is stored in EPROM (Erasable Programmable Read Only Memory).
The Random Access Memory (RAM) is used by the microprocessor e.g. for temporary storage of data.
The control bus is running signals to control and select the parts in the circuitry.
These signals are decoded out of the address bus by the Decoders (D2323, D2321 And D2311).

Pushbuttons interface
The information which is applied to the analyzer by operating the selection-pushbuttons is via pushbutton interface circuitry set on the data bus. The microprocessor assimilates this information and, if necessary, takes action.

Interface oscilloscope
In the analyzer mode the information to be displayed is, via this interface circuit applied, to the deflection circuitry of the oscilloscope. The interface takes care of the character generation and the horizontal deflection and the vertical deflection.

Pod´s
Three PM 8821 pod´s are connected to the system under test.
Data, clocks and clockqualifiers are via these pod´s applied to the state-analyzer.

Data delay
In order to keep the hold time zero the captured data is delayed in respect to clocks and clock-qualifiers signals.

Data Input Latches
The input data must be latched to be sure that data is stable during the write cycle of the Data Acquisition Memory.

Data Acquisition Memory
The captured data is written in the Data Acquisition Memory. The contents of the Data Acquisition Memory is displayed on the screen after the data acquisition is stopped.

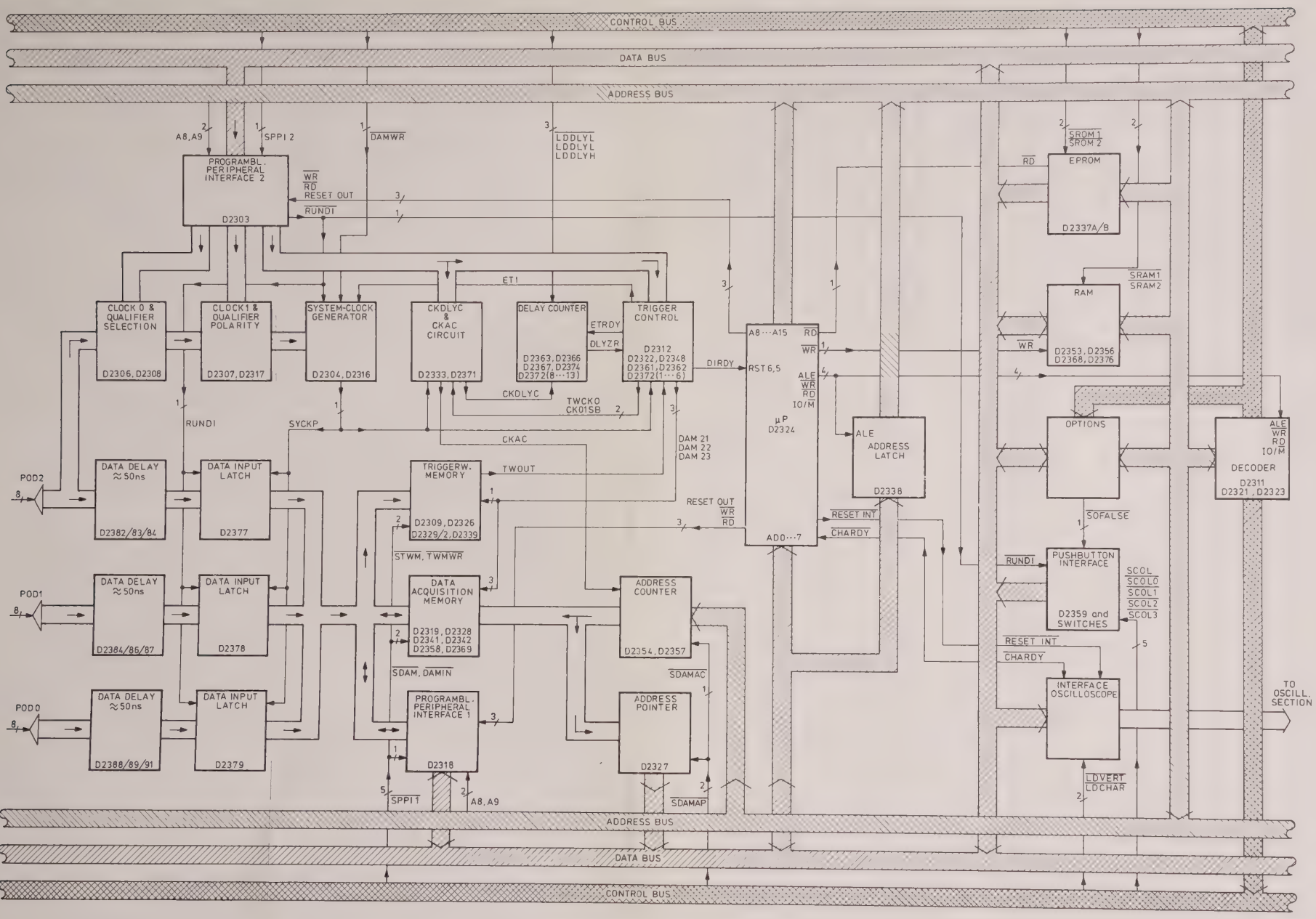


Fig. 1.5. Block diagram of the state analyzer part PM 3543

MA10453

Address Counter
The Data Acquisition Memory is addressed by the Address Counter.
The uP can load the Address Counter via the data bus with every initial value.

Address Pointer
When the Data Acquisition has been stopped the microprocessor reads the value of the address counter via the Address Pointer.

PPI 1 - Programmable Peripheral Interface 1
PPI 1 connects the Data Acquisition Memory and the Triggerword Memory with the data bus. The microprocessor reads the contents of the Data Qcquisition Memory using PPl as an input port.
The microprocessor writes the triggerwords in the Triggerword Memory and status information in the Data Acquisition Memory by using PPIl an output port.

Triggerword Memory
Before starting the data acquisition a trigger combination must be selected. The selected combination is via the pushbutton Interface, the data bus and PPI 1, under control of the microprocessor, written in the Triggerword Memory. When after starting the data acquisition the trigger combination is found, the Triggerword Memory gives a signal to the Trigger control circuit which takes care of further actions.

PPI 2 - Programmable Peripheral Interface 2
PPI 2 is programmed as an output port for the microprocessor.
This PPI connects the data bus with
- the clock and qualifier selection circuit,
- the clock and qualifier polarity circuit,
- the system clock generator and
- the trigger control circuit.
These circuits are controlled by the microprocessor via the data bus and output port PPI 2.

Clock and clock-qualifier selection
The selected clocks and clock-qualifier inputs are enabled by control signals from the microprocessor.

Clock and clock-qualifier polarity
The selected edges and levels of clock-and clock-qualifier signals are applied to the System clock generator.

Systemclock generator
The Systemclock generator shapes the systemclock pulse (SYCKP) out of the clock-and clock-qualifier signals received from the Clock and Clock-qualifier circuit.
Essential parts of the analyzer, e.g. the Data Input Latches and the Trigger Control circuit, operate under control of the systemclock.

Clock Delay Counter (CKDLYC) and Clock Addres Counter (CKAC) circuit
This circuit generates CKDLYC and CKAC out of the Systemclock.

The Address Counter can be incremented by clock states or by triggerword recognitions.
The Delay Counter can be decremented by clock-states or triggerword recognitions.

Delay Counter
When the trigger condition is found data acquisition is stopped. Stopping the data acquisition can be delayed by a pre-selected number of clock states or trigger combinations. This selected delay is loaded in the Delay Counter. When the selected delay has been counted down to zero the Trigger Control circuit is informed and data acquisition is stopped .

Trigger Control circuit
The Trigger Control circuit controls the data acquisition for the different trigger modes. The trigger modes parallel. quasi-parallel, sequential, immediate sequential and the trigger delay can be selected by means of the front panel pushbuttons. This information is via the Pushbutton Interface, the data bus and Programmable Peripheral Interface 2 offered to the Trigger Control circuit.

1.4.2. Oscilloscope part (see Figure 1.6.)

Y-Channel

The vertical channels A and B for the signals to be displayed are identical, each comprising an input coupling switch, an input step attenuator, an impedance converter and a preamplifier with trigger pick-off.
A channel multivribrator, controlled by the display mode pushbuttons, switches either channel A or channel B to the final Y amplifier via the delay line. The channel multivibrator is operated by a pulse at the end of the sweep, and offer uninterrupted display of the A and B waveforms in the ALT mode. In the CHOP mode the multivibrator is free-running and provides a chopped display of the two signals. In the ADD position, both switching amplifiers (PULL TO INVERT B) the A-B mode is obtained.

The AMPL/DIV switches provide x1 or x10 gain control of the preamplifier, which offers in conjunction with the step attenuator a full range of deflection coefficients in a 1-2-5 sequence.

Triggering

To initiates sweeps, trigger signals can be derived from the A and B vertical channel preamplifiers, from an external source, or internally from the analyzer part as selected by the trigger source switch. With A and B pushbuttons both depressed, composite triggering is derived from the delay-line drive stage. The polarity of the trigger signal, negative or positive-going, on which the display will start is determined by changing the output polarity of the impedance converter.

With the AUTO switch depressed, the peak-to-peak level detector comes into operation. The peak-to-peak level of the signal then determines the range of the LEVEL control.

With AC or DC depressed, the range of the LEVEL control is fixed.

In the TV mode the LEVEL control is inoperative and the TV sync separator is switched into circuit, thus initiating sweeps with line or frame pulses as dictated by the setting of the TIME/DIV switch.

Time-base circuit

For normal internal time-base operation the horizontal amplifier is fed by sweeps from the time-base circuit.

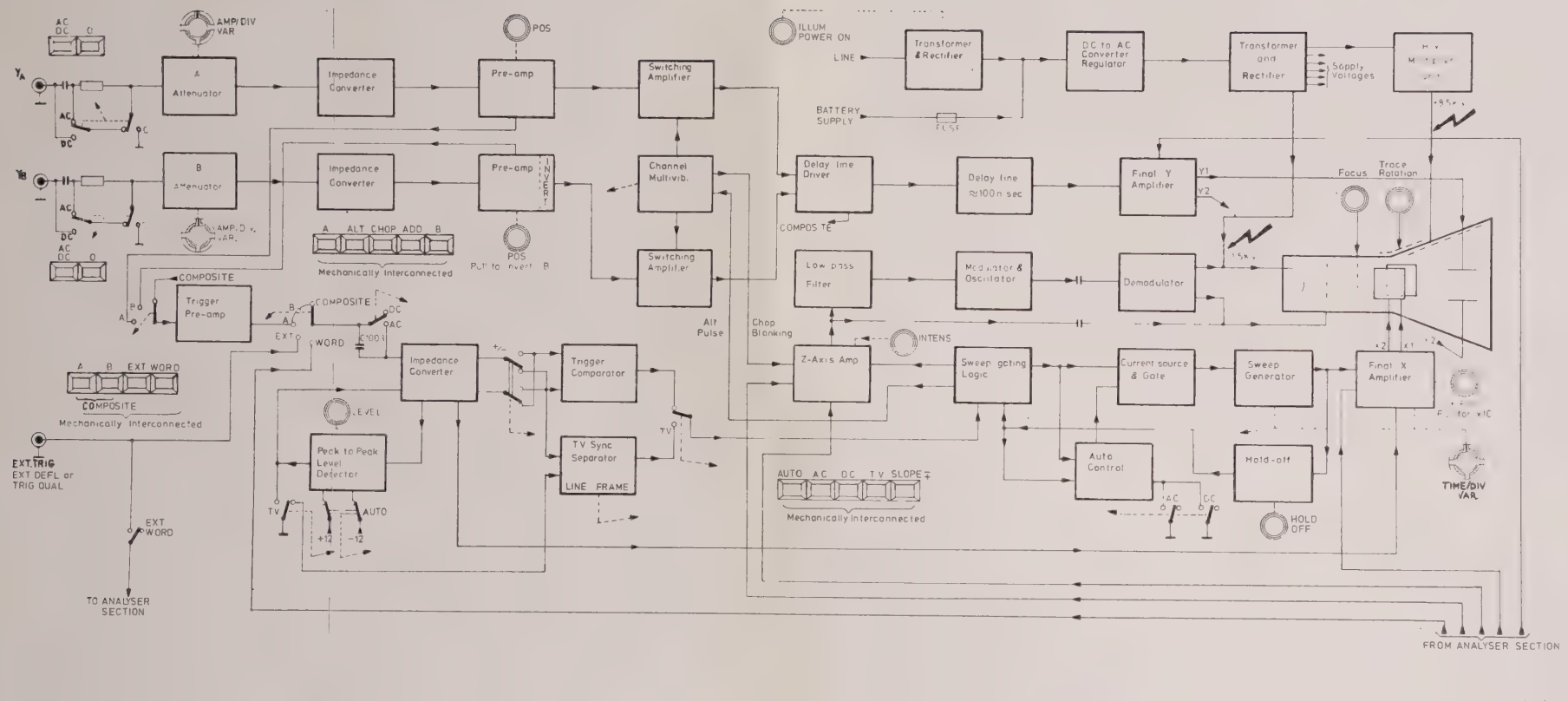


Fig. 1.6. Block diagram of the oscilloscope part

With AUTO depressed, in the absence of trigger signals, the output of the sweep generator is fed back via the hold-off circuit and gate to its input. This causes sweeps to free-run and a resultant trace is displayed on the screen. As soon as the AUTO control circuit detects a trigger (i.e. change in the output of the sweep-gating logic) the sweep is fed back to the sweep-gating logic. This causes the circuit to revert to the normal triggering mode in which sweeps are initiated only by trigger pulses at the input of the sweep-gating logic.

With AC or DC depressed, AUTO control is made inoperative. Sweeps are then only produced provided a trigger signal is present and the LEVEL control appropriately set. The display can be magnified in the horizontal direction by increasing the gain of the final amplifier.

In the X-DEFL position of the TIME/DIV switch, the sweep generator output to the final amplifier is inhibited and the impedance convertor is connected directly to the final amplifier. In this way, the signals normally selected for triggering, or an external source, can now be used for horizontal deflection.

Hold-off circuit

The hold-off stage, as its name implies, "holds-off" triggers from the input of the time-base circuit until the trace has completely returned and the time-base circuits are completely reset. The hold-off time can be increased by turning the HOLD-OFF control clockwise.

Z-Axis

The Z amplifier provides for the blanking of the trace during the fly-back and hold-off time. In addition, it blanks the sweep in the CHOP mode during the switching transients. Moreover the trace can be blanked by a signal applied to the external Z-mode input.The l.f. components of the blanking signal are modulated and demodulated before they are applied to the Wehnelt cylinder together with the a.c. coupled h.f. components.

Power supply

The mains (line) supply is transformed and rectified before being applied to a d.c. to a.c. converter. When the instrument is operated from a battery supply the battery output is connected directly to the d.c. to a.c. converter.
The output of the converter is coupled to a transformer and rectifier which, after rectification, provides the - 1.5 kV e.h.t. potential and the circuit supply voltages. The - 1.5 kV is also multiplied to 8.5 kV to supply the required total accelerating voltage of approx. 10 kV.

2. CIRCUIT DESCRIPTION

2.1. Description of the State Analyzer part

2.1.1. General Information

In this Chapter the circuit description of the Logic Scope PM 3543 is given.
The PM 3542 differs as per the following details :

Hardware differences

Data acquisition circuitry :
Only two pods can be connected.
Pod 1 : data 0-7
Pod 2 : data 8-10
clockqualifier Q2/data 11
clockqualifier Q1/data 12
clockqualifier Q0
clock CK1
clock CK0
Not present components : X12, D2388, D2389, D2391, D2379, D2358, D2369, D2339 and associated resistors and capacitors

Memories :
The promset D2337 A + B of the PM 3542 consists of one 2732 and one 2716 EPROM while the promset of the PM 3543 consists of two 2732 EPROM´s.

Software differences

There is a great difference in the software contents of the PM 3542 and and PM 3543
The software controls the whole scale of operations of the logic scope.

2.1.2. Data acquisition circuit (See Figure 7.5.)

2.1.2.1. Threshold adjusting

These threshold levels TTL, VAR 1 and VAR 2 can be selected by tumbler switch S39 (THRESHOLD) on the front panel. The selected threshold can be checked on measuring pins X14 and X15 (connected to resp. X 2306 and X 2304) and the reference voltage U REF is applied to the Logic Pod´s.
TTL : fixed level
VAR 1: threshold level can be selected between -3 V to +12 V by potmeter R16
VAR 2: threshold level can be selected between -3 V to +12 V by potmeter R17

2.1.2.2. Data capturing

The Logic Scope is connected to the System Under Test (SUT) via three Logic Pod's PM 8821. The connections of the pod's to the SUT are:
Pod 0: 0-7 : data D0-D7
Pod 1: 0-7 : data D8-D15
Pod 2: 0-2 : data D16-D18
3 : Q2/data D19
4 : Q1/data D20
5 : Q0/
6 : clock CK 1
7 : clock CK0
Pod 2 is connected to X 11
Pod 1 is connected to X 12
Pod 0 is connected to X 13

Clocks and clock-qualifier signals are applied to the clock and clock-qualifier circuit.
The clock-qualifier inputs Q1 and Q2 are interchangeable with data inputs D19 and D20.
In order to keep the hold time at zero data is delayed relative to clock and clock-qualifier signals. The hold time is the time that data must be present at the input before it is captured. Data is delayed by two RC-networks. The levels and edges of the signals input are adjusted by two inverters (D2382/83/84/87/88/89/91). See figure 7.5. "Data acquisition circuit".

During the data acquisition ($\overline{RUNDI}$ = 0) is latched in the Data Input Latches on the leading edge of the SYCKP.
When the control signal $\overline{RUNDI}$ = 1 the outputs of the Data Input Latches are disabled.

2.1.2.3. Data Acquisition Memories D2319/28/41/42/58/69

Data is stored in the Data Acquisition Memories (DAM).
The DAM's consist of six 256x4 bits Random Access Memories, D2319, D2328, D2341, D2342, D2358, D2369.
The DAM's are selected by the signal $\overline{SDAM}$. Data latched in the Data Input Latches is written in the DAM when $\overline{DAMIN}$ is 1 and SYCKP is 0. The data is written on the location addressed by the Address Counter.
255x21 bits of the DAM are used for storage of data.
At each word are three bits added (DAM 21, 22, 23) containing information about the status. See chapter 2.1.3.3.
When data acquisition is stopped the DAM's are read by the microprocessor using PPI 1 as an input port (see chapter 2.1.2.6.). Therefore $\overline{SDAM}$ and $\overline{DAMIN}$ must be a 0 and SYCKP must be a 1.

2.1.2.4. Address counter D2354 - D2357

The locations in the DAM are during data acquisition, addressed by the Address Counter. The Address Counter consists of two 74LS191 binary counters, D2354 and D2357. The Clock signal CKAC is generated out of the Systemclock (SYCKP). See chapter 2.1.4.2.
When the least significant counter D 2357 overflows (1111 to 0000), the most significant counter D2354 is enabled. The Address Counter counts from 0 to 255.
When data acquisition is stopped the contents of the DAM is displayed on the screen. The address in the DAM which must be read, is by the microprocessor, via the address bus loaded in the Address Counter. When SDAMAC is 0, the outputs of the Address Counter will follow the inputs regardless the clock-input.
Via the Address Pointer the microprocessor reads the value of the Address Counter when the data acquisition is stopped.

2.1.2.5. Triggerword Memories (D2309/26/39)

Before data acquisition is started the triggerword or triggerwords are written in the Triggerword Memories, which consist of three 256x1 bits Random Access Memories.
The Triggerword Memories are written by the microprocessor, using PPI 1 as an output port, when $\overline{\text{STWM}}$ and $\overline{\text{TWMWR}}$ are 0.
On the locations which address matche the triggerword value a "0" is written. On all the other locations a "1" is written.
The maximum size of the triggerword is 21-bits. Two triggerwords can be recognized by the Triggerword Memory. The difference between the first and the second triggerword is indicated by DAM 21, which is connected to the most significant address input of each Triggerword Memory. The first triggerword addresses the least significant half of the Triggerwort Memory (DAM 21) and the second the most significant half).
When data acquisition is started the microprocessor sets $\overline{\text{TWMWR}}$ to 1 and $\overline{\text{STWM}}$ to 0 and the Triggerword Memories are read.
When a triggerword is recognized TWOUT becomes 1. This signal is applied to the Trigger Control Circuitry. (See chapter 2.1.4.1.).

2.1.2.6. Programmable Peripheral Interface - PPI 1 (D2318)

PPI 1, P8255A, is selected if SPPI 1 is 0. In case the PPI is not selected the output is disconnected from the data bus.
The status of the PPI is determined by a controlword written in the PPI when address lines A8 and A9 are 1.
For reading the DAM´s the ports PA, PB and PC are all used as input ports for the microprocessor. See Fig. 7.5.

For loading the Triggerword Memories ports PA, PB and PC must all be used as output ports for the microprocessor. This status is determined by another controlword set on the data bus when A8 and A9 are 1. See Fig. 7.5. After the triggerword values have been written to the output ports the Triggerword Memories are loaded by making $\overline{STWM}$ and $\overline{TWMWR}$ 0.

2.1.3. Clock and clock qualifier circuit

2.1.3.1. Selection and polarity

Clocks and clock-qualifiers can be selected with the pushbuttons on the frontpanel of the analyzer. This information is applied to the microprocessor which generates the belonging selection signals. These signals are written in the Programmable Peripheral Interface/2.

PPI 2 is selected by the low-active signal SPPI/2. When this signal is 1 the input of the PPI is switched of from the databus. The status of the PPI is determined by a controlword set in the PPI, via the databus, when addresslines A0 and A1 are 1. The ports PA, PB and PC are in this configuration all used as output-ports and can be selected and written as shown in fig. 2.5. (Memory map) When the status of the PPI is determined, selection signals are written in the ports PA, PB and PC. These selection signals are continuously available at the outputs of the ports until they are changed by the microprocessor.
The selection signals of clock CK0 and belonging qualifiers are available at port PA and the selection signals of clock CK1 and belonging qualifiers at port PBA. Clock or clock-qualifier is selected if the belonging selection signal is 1. Then the selected signal passes the SELECTION NAND-gate (D2308, 2306) is inverted and fed to the POLARITY EXCLUSIVE-OR-gates. Clock CK0, the main clock must always selected, so the input of its belonging NAND-gate is connected to +5 V. The polarity of clocks and clock-qualifiers is determined by the POLARITY EXCLUSIVE-OR-gates (D2317, D2307). See table with selection signals.

2.1.3.2. Systemclock generation (See fig. 7.6.)

The signal ETI must be 1 to enable Systemclock generation out of the applied clocksignals.
Reading the contents of the DAM´s the microprocessor can distinguish valid and unvalid data by the status bit DAM23. Before the data acquisition started DAM23 is made a 1 (= unvalid) on all the memory locations of the DAM D2319. The necessary SCYCKP is generated by means of a pulsing $\overline{DAMWR}$ signal. During data acquisition $\overline{DAMWR}$ is 1 and the microprocessor makes control signal $\overline{RUNDI}$ 0 which enables systemclock generation.

Output (8) of D2314 becomes a 0 (because $\overline{Q}$ outputs of the FF´s D2304 are already a 1) and data acquisition can start. When no clock-qualifiers are selected or the selected clock-qualifiers are true, outputs 8 and 6 of NAND-gates D2316 are 1. Assume that the first received clocksignal is CK0 and the

selected polarity is 1. That means that at the first positive going edge of CK0 output $\overline{Q}$ (9) of FF D2304 becomes a 1 and Q (8) becomes a 0. The inverted output signal $\overline{Q}$ is applied to NAND-gate D2314 which output (8) becomes 1. Output $\overline{Q}$ (6) of D2304 is 1 because there is no CK1 received.

On the first positive going edge of CK0 the output (8) of D2314, SYCKP, becomes a 1. On this edge data is latched into the Data Input Latches.
SYCKP is inverted by INVERTER D2302 and delayed by the delay circuitry consisting of 4 OR-gates D2381 and RC-combinations. The inverted and delayed SYCKP is called $\overline{\text{RSYCKP}}$ and resets the FF's D2304 and therefore the SYCKP.
$\overline{\text{RSYCKP}}$ becomes 1 again and the next SYCKP can be generated. The generation of SYCKP out of CK1 is identical.

2.1.3.3. Clock and data identification

The microprocessor needs the following information about each captured and stored word :
- is the captured word valid;
- is the word captured with CK0 or CK1 and
- is the first triggerword already found?

This information, stored in three bits, DAM 23, DAM 22 and DAM 21, is added to every stored data word and is composed by multiplexer D2322. This multiplexer is enabled during data acquisition (i.e. $\overline{\text{RUNDI}}$ = 0 and ETI = 1).
DAM 21 : TWCK0 indicates if the first triggerword, always captured by CK0 has been found. TWCK0 is 1 if the triggerword is found and is 0 if the triggerword is not yet found.
DAM 22 : CK1 SB = 1 : data word has been captured by CK1. FF D2312 is set (12) by a SYCKP generated by CK1.
CK1 SB = 0 : data word has been captured by CK0. FF D2312 is reset (10) by a SYCKP generated by CK0.
DAM 23 : $\overline{\text{VADIB}}$: in combination with DAM 22 used to inform the microprocessor if a data word stored in the DAM is valid or invalid. These conditions can be different for each triggermode.
The microprocessor uses the information stored in these three bits to calculate the line number which is displayed in front of the data on the screen.

2.1.4. Trigger Control circuit

2.1.4.1. Trigger mode circuit (See Fig. 7.6.)

Two dual 4 to 1 line multiplexers, D2348 and D2361, and one dual FF, D2362 are the main elements of the Trigger Control circuit.
To give the required triggermode the selection signals SMPX0 and SMPX1 have the values as shown in the tabel of figure 2.1.
These signals are controlled by microprocessor and via PPI 2 applied to the multiplexers.

The function of the controlsignal CKO1SB is to indicate if the second triggerword is captured with selected clock. CKO1SB is controlled by 2 to 1 multiplexer D2322.
The control signal STWCKO indicates if the second triggerword must be captured with CKO or CK1.
Two modes can be distinguished:
- STWCKO = 1: second triggerword must be captured with CKO
  CKO1SB = 1: data captured with CKO
  CKO1SB = 0: data captured with CK1
- STWCKO = 0: second triggerword must be captured with CK1
  CKO1SB = 1: data captured with CK1
  CKO1SB = 0: data captured with CKO

The selection signal STWCKO controlled by the microprocessor and via output port PA of PPI 2 applied to multiplexer D2322.

When the parameters are set the microprocessor first sets RUNDI 1 via data bus and PPI 2.
Secondly the microprocessor generates via address bus and decoder D2312 an active low $\overline{\text{STRDI}}$ puls. The positive edge of this puls sets the output (5) of FF D2372, ETI to 1, by which generating of SYCKP is enabled and data acquisition can start.
If the triggermode "false" is not selected input (10) of EXCLUSIVE-OR-gate D2331 is 0 (See also the part "false triggering" in this Chapter).
The Triggermode circuit is described for 5 triggermodes seperately, assuming that there is no external trigger qualifier selected.

	SMPX1	SMPX0
parallel triggering	0	0
Quasi-parallel triggering	0	1
immediate sequential triggering	0	1
sequential triggering	1	0
sequential triggering with intermediate delay	1	1

Fig. 2.1. Tabel of triggermode selection signals.

Parallel trigger mode
SMPX0 = 0 and SMPX1 = 0
Only one triggerword and one clock, CKO, are selected. The selection signals SMPX0 and SMPX1 are both 0 so the input numbers "0" of multiplexers D2348 and D2361 are selected.
After the Delay Counter has been loaded LDDLYL becomes a 0 by which FF D2362 is set and multiplexer D2348 is enabled.
Untill the selected triggerword is recognized TWOUT stays 0,

and output (6) of NAND-gate D2314 remains 1.
TWCKO is by multiplexer D 2361 applied to NAND-gate D2364. The output (8) of this NAND-gate stays a 1, ETI remains a 1, and data acquisition is continued until the triggerword is recognized.
When the triggerword is recognized TWOUT becomes a 1. CKOS is a 0 because data is captured with CKO. Therefore output (6) of NAND-gate D2314 becomes a 0.
Output (9) of FF D2362 becomes 0 at the next positive going edge of SYCKP. This output signal is by multiplexer D2348 applied to the active low reset (13) input of FF D2362 and the FF is "locked" in the present condition. The inverted output (8), TWCKO, becomes a 1 and enables the Delay Counter by signal ETRDLY. When the delay has been counted down to 0 or when no delay was selected the signal DLYZR becomes a 1.
Then output (8) of NAND-gate D2364 becomes 0, and FF D2372 is reset. ETI becomes a 0 and SYCKP generation is disabled so that data acquisistion is stopped. The signal DIRDY interrupts the microprocessor by its RST6,5 input and the display subroutine is entered. After the triggerword is recognized and the selected delay has been counted down to zero data acquisition is stopped.
Triggerword recognition and stopping the data acquisition takes one SYCKP so before data acquisition is stopped another word is stored in the DAM.This invalid last word is not displayed on the screen.

Quasi-parallel trigger mode
SMPXO = 1 and SMPX1 = 0
Two triggerwords selected Triggering occurs when immediately after the first triggerword, with CKO, the second is found, with CK1.
TW OUT becomes a 1 if the first triggerword is found. ETI and CKOS are 1 so output (6) of NAND-gate D2314 becomes a 0.
On the next positive going SYCKP the inverted output (8), TWCKO, of FF D2362 becomes a 1.
TWOUT stays 1, if the next captured word matches the second triggerword, but output (6) of NAND-gate D2314 becomes a 1 because CKOS has become a 0. Besides FF D2362 is not "locked" now.
Because CKO1SB and TWOUT remain a 1 the output (12) of NAND-gate D2314 becomes a 0.
On the next positive going edge of SYCKP the inverted output of FF D2362 becomes a 1 by which, via multiplexer D2361, the Delay Counter is enabled. Output (5) of FF D2362 has become a 0. The FF is "locked" in this condition. The delay can be counted down to zero and data acquisition can be stopped. The last captured word is invalid and not displayed on the screen.

Immediate sequential trigger mode
SMPXO = 1 And SMPX1 = 0.
Two trigger words selected.
Triggering occurs if immediately after the first triggerword, on CKO, the second is found on CKO.
When the first triggerword is found TWOUT becomes 1 and therefore the output (6) of NAND-gate D2314 becomes a 0. On the next positive going edge of SYCKP the inverted output (8), TWCKO, of FF D2362 becomes a 1. When the second triggerword is found immediately on the next selected edge of CKO, TWOUT and

CK01SB remain 1, so output (12) of NAND-gate D2314 becomes a 0.
On the next positive going edge of SYCKP the inverted output (6) of FF D2362, which enables the Delay Counter (ETRDLY becomes a 1).
Data acquisition is stopped when the selected delay has been counted down to zero.
The last captured, invalid, word is not displayed on the screen.

Sequential trigger
SMPX0 = 0 and SMPX1 = 1.
Two triggerwords selected. After the first triggerword is captured with CK0, the second triggerword must be captured with selected CK0 or CK1. No delay selected between the triggerwords.
When the first triggerword is recognized output (6) of NAND-gate D2314 becomes a 0. On the next positive going edge of SYCKP the inverted output (8) of FF D2362, TWCK0, becomes 1.
Output (9) of this FF is connected to its active low reset input, so the FF is "locked" in this condition.
When the second triggerword is found TWOUT becomes a 1 again, and output (12) of NAND-gate D2314 becomes a 0 if the second triggerword is captured with selected clock. (CK01SB is 1).
On the next positive going edge of SYCKP the inverted output (6) of FF D2362 becomes a 1 and the Delay Counter is enabled (ETRDLY=1). The FF is locked in this condition. After counting the Delay Counter to 0, on the clock selected with the second triggerword, ETI becomes a 0 and generation of SYCKP is disabled data acquisition is stopped.
The last captured, invalid, word is not displayed on the screen.

Sequential trigger mode with delay selected between the triggerwords
SMOX0 = 1 and SMOX1 = 1.
When the first triggerword has been found, on CK0 and the selected delay has been counted down to 0, on the clock selected with the second triggerword, the second triggerword must be found, on selected CK0 or CK1.
Output (6) of NAND-gate D2314 becomes 0 when the first triggerword is found. On the next positive going edge of SYCKP the inverted output (8), TWCK0, of FF D2362 becomes 1. The FF is "locked" in this condition. The Delay Counter is enabled and counted down to zero on the clock selected with the second triggerword. When the Delay Counter reaches 0 DLYZR becomes 1. At that moment searching for the second triggerword starts.
The preceding operation is identical to the earlier described sequential trigger mode without delay between the triggerwords.

False triggering
False triggering can only be selected on the second triggerword, in quasi-parallel, sequential, sequential with delay and immediate sequential trigger mode.
When false triggering is selected control signal $\overline{\text{ROW3}}$ is 0.
When the analyzer searches for the first triggerword output (9) of FF D2362 is 1 and the signal $\overline{\text{ROW3}}$ is ignored.
If the analyzer searches for the second triggerword output (9) of FF D2362 is 0 and output (10) of NAND-gate D2302 a 1. Now output (8) of EXCLUSIVE-OR-gate

D2331 becomes a 1 if TWOUT becomes 0. TWOUT becomes 0 when the captured data word doesnot match the selected triggerword. In that case data acquisition is stopped.
NOTE: However the second triggerword must be false the clock selected with this triggerword must be true.

2.1.4.2. Generation of Clock Address counter signal (CKAC), See figure 2.2.

MUX 2 (address counter clock)				
Enable 2 SKYDA	SCYDLY	TWCKO	CKAC	Selected MUX input
1	X	X	S clock	None
0	X	0	T clock	4&6 (first Trigger Word)
0	X	1	T clock	3&5 (sec. Trigger Word)

Fig. 2.2. Generation of the signal Clock Address counter

Data captured on clockstates : "DATA=S"

Data is captured on clockstates if the microprocessor control signal SCYDA is 1. This signal is applied to the enable input of dual 4 to 1 multiplexer D2333/2. The associated 4 to 1 multiplexer is disabled and the output (7) becomes a 0.
The inverting output (8) of FF D2371, CKAC, becomes a 1 every positive going edge of SYCKP and a 0 again by the signal $\overline{\text{RSYCKP}}$ on the Set input (10) of this FF. On each positive going edge of SYCKP the next location of the DAM is addressed by the Address Counter.

Data captured on triggerrecognitions: "DATA=T" (only triggerwords captured)

Only triggerwords are captured if multiplexer D2333/2 is enabled by SCYDA is 0.
- Parallel and sequential trigger mode.
When the analyzer is looking for a triggerword, TWCKO is 0 and inputs 0 (6) or 2 (4) of multiplexer D2333 are selected.
When a triggerword is found output (6) of NAND-gate D2314 becomes a 0 and on the next positive going edge of SYCKP signal, CKAC and TWCKO become a 1.
FF D2362 is locked in this condition, flip-flop D2371 (10) is resetted by $\overline{\text{RSYCKP}}$.
After the first triggerword is found inputs 1 (5) or 3 (3) of multiplexer D2333 are selected (because signal TWCKO has become a "1"). Following triggerwords that are found make output (12) of NAND-gate D2314 a 0 and the Address Counter is incremented by CKAC

- quasi-parallel and immediate sequential trigger mode.
When the analyzer finds the first triggerword CKAC is activated, and finding

the second triggerword immediately after that CKAC is activated again. If the second triggerword is not immediately found after the first the analyzer starts looking again for the first triggerword.

2.1.4.3. Generation of Clock Delay Counter signal (CKDLYC), See figure 2.3.

MUX 1 (delay counter clock)				
Enable 1	SCYOLY	TWCKO	CKDLYC	Selected MUX input
0	0	0	No CLock	10
0	0	1	T Clock	11
0	1	X	S Clock	12 & 13

Fig. 2.3. Generation of the signal Clock Delay Counter

Delay counter counted down by clockstates: "DLY=.....S"

The Delay Counter is decremented by clockstates if controlsignal SCYDLY is a 1. The output signal (6) of EXCLUSIVE-OR-gate D2331 is 0 when CKO1SB is 1. CKO1SB is 1 if data is captured with the clock, CK0 or CK1, selected in combination with the second triggerword or, in the parallel mode, when data is captured with CK0. Therefore in quasi-parallel and sequential trigger modes the selected delay is always counted down by the clock selected with the second triggerword.

Delay counted down by triggerword recognitions: "DLY=.....T"

In this mode signal SCYDLY is 0.
When the triggerword is not yet recognized TWCK0 is 0, input 0 (10) of multiplexer D2333/1 is selected. Output (9) of this multiplexer is "connected" to 1 (+5V) and no CKDLYC is generated.
One SYCKP after the triggerword is recognized TWCK0 becomes a 1 and the output (9) of the multiplexer is "connected" to output (12) of NAND-gate D2314. With the next recognized triggerword the output (12) of NAND-gate D2314 becomes a 0 and the next positive going edge of SYCKP decrements the Delay Counter by CKDLYC.

2.1.4.4. Delay Counter

The Delay Counter consists of three HEF 4029BP counters and one 74LS191 counter. These four 4-bit counters allow a maximum delay of 65535.
Before data acquisition is started the two most significant counters D2367 and D2374 are loaded via the data bus under control of the signal LDDLYH.
After that the two least significant counters D2363 and D2366 are loaded under control of the signals $\overline{\text{LDDLYL}}$ and LDDLYL. The counters are hardware programmed to count down. The clock input of the least significant counter

D2366 is connected to the CKDLYC signal. The clock inputs of counters D2367 and D2374 are connected to the active low TC outputs of D2374 and D2363 respectively.
D2367, D2374 and D2363 are enabled via the signal $\overline{\text{RUNDI}}$ which becomes 0 when data acquisition is started.
D2366 is enabled by the signal $\overline{\text{EDLYC}}$ which is 0 if ETRDLY and $\overline{\text{DLYZR}}$ become 1. Depending the trigger mode the trigger delay can be selected after recognition of the first or the second triggerword.
When the triggerword, after which the delay is selected, is recognized it takes one SYCKP before ETRDLY becomes a 1.
D2372 has been reset by ETRDLY is 0 so $\overline{\text{DLYZR}}$ is already 1. After ETRDLY has becomes 1 output (6) of NAND-gate D2364, $\overline{\text{EDLYC}}$ becomes 0, which enables D2366. The next positive going edge of CKDLYC decrements the Delay Counter.
When D2366 has reached 0000 the TC output (12) becomes 1. The outputs of D2366 become 1111 on the next positive going edge of CKDLYC. The positive going edge of the most significant bit is used as a clock for D2363. When 2363 reaches 0000 the $\overline{\text{TC}}$ output (7) becomes 0. On the next clockpulse from D2366 the output of this counter becomes 1111 and the $\overline{\text{TC}}$ output (7) becomes 1 again. This positive going edge is used as a clock for D2374 and so on.
One clock state before the Delay Counters reach zero the outputs of all NAND-gates D2373 become 1. This signal is applied to the D-input (12) of FF D2372. Output (9) of FF D2372 becomes a 1 on the next positive going edge of CKDLYC. The FF is locked in this condition via the set input (10).
Because DLYZR becomes 1 and the output (9) of multiplexer D2361 is 1 output (8) of NAND-gate D2364, becomes 0 and FF D2372 is reset. ETI becomes 0, so generation of SYCKP is stopped and DIRDY becomes 1 by which the microprocessor (via input RST6,5) is informed about the end of data acquisition. $\overline{\text{DLYZR}}$ becomes 0, output (6) of NAND-gate D2364, $\overline{\text{EDLYC}}$ becomes 1 and the Delay Counter is disabled.

2.1.4.5. TRIG OUT and TRIG IN (Sockets X8 and X10)

If data acquisition is ready (DIRDY is 1) output (11) of NAND-gate D2364 gets 0 and the level of TRIG OUT becomes a 1.
This signal is applied to a BNC-socket at the rear side of the logic scope which can be used for triggering of other equipment. Via TRIG IN, BNC-socket on the rear side of the instrument, the analyzer can be triggered externally.
This signal is latched in D2377 and applied to 4 to 1 multiplexer D2344 and NAND-gate D2313. When the analyzer is not externally triggered, that means that the external trigger signal is still zero, TWINS remains 0. Output (3) of NAND-gate D2313 stays 1 so the differential comparator D2329/2 is strobed. The output of multiplexer D2344 is 1 so the output of comparator D2329/2, TWINS becomes a 1 if the analyzer is externally triggered or when no device is connected to the TRIG IN BNC-socket.
The output (3) of NAND-gate D2313 becomes 0, at least when no triggerqualifier is selected, and comparator D2329/2 is disabled, which means that the output becomes a 1. This control signal indicates that the analyzer can be triggered if the trigger conditions are true.

2.1.4.6. External Triggerqualifier (socket x5) and TRIG.IN (X10)

An External Triggerqualifier signal can be connected, via an oscilloscope probe to the BNC,connector (X5) TRIG QUAL at the front panel. This triggerqualifier is active if the pushbuttons WORD and EXT are depressed simultaneously. The triggerqualifier can be selected "0" or "1" and can qualify both triggerwords (an unused input is regarded as a "0" and thus the signals QTWIN and QTWINS are "0").
This is controlled by the microsprocessor by means of the control signals SQTW1 and SQTW2.
Depending the selected polarity the control signal PQTW is 1 or 0. The triggerqualifier signal QTWIN is successively adjusted, delayed and latched in the Data Input Latch D2377.
If no external TRIG IN via X10 is connected TWINS is 1 (the open input is regarded as a "1"). TWCKO is 0 when the analyzer is searching for the first triggerword so input 12 (number 2) of multiplexer D2344 is "selected" which indicates by means of SQTW1, that the external triggerqualifier is selected on the first triggerword.
When the external triggerqualifier is selected the output of D2344 becomes a 1. Suppose the selected polarity is 0, that means that output (3) of EXCLUSIVE-OR-gate D2331 is 1. When the trigger qualifier is 0, signal QTWINS is 0 so output 11 of EX- OR D2331 is 1 this means that the outputs of NAND-gate D2313 is 0 (both inputs are 1) and the output (9) of comparator D2329/2 is true (i.e. "1"). This means that TWOUT is 1 and the combination TRIG IN and Triggerqualifier is true. If the Triggerqualifier doesnot match the selected polarity the comparator output not true (o) and TWOUT is 0.
After the first triggerword is found TWCKO is 1 and input 13 (number 3), SQTW2, of multiplexer D2344 is "selected" being the selection signal for the qualifier on the second triggerword.

2.1.4.7. Combi mode

In the combi mode the oscilloscope is triggered by the analyzer. The combi mode is selected when WORD is depressed. By pressing WORD relais K2501 is activated and the analyzer is connected to the oscilloscope.
The signal DIRDY, which becomes a 1 if the data input is ready, is via NAND-gate D2364 and connectors X2313 and X2501 applied to the PC-board WORD. Transistor V501 is connected to the trigger section of the oscilloscope. The oscilloscope triggers when the transistor conducts, so when DIRDY becomes a 1. If WORD is not depressed there is no connection between the analyzer and the oscilloscope´s trigger circuit.

2.1.5. Interface oscilloscope (See fig.7.9.)

The interface oscilloscope circuit transforms the output of the analyzer into a suitable input signal for the oscilloscope deflection circuit to produce a visual display of selected parameters and captured data on the CRT.

2.1.5.1. Character generation

The ASCII (American Standard Code for Information Interchange) characters are stored in EPROM D2104. Each character is stored in 8 memory locations of 8-bits each. See Fig.2.4.
The 1´s represent the character on the screen.
The Character Generator is enabled when the signal SWLZ is 0.
This signal is 0 when the analyzer mode is selected.
SWLZ is 1 if the oscilloscope mode is selected; then the output of the Character Generator is high impedance.
The memory location in which a character is stored is selected by the address inputs A3...A8 of the Character Generator.
This address is by the microprocessor, via the data bus latched in the ASCII Latches D2112 and D2111 when the signal $\overline{\text{ENASC}}$ is 0. The 8-bit words representing the column of the character are addressed with the least significant address inputs A0..A2 on the Character Generator. These columns are addressed by the 47-counter D2116 and D2108.
NOTICE: Only 64 characters have to be stored so the address lines A9 and A10 are connected to ground. That means that the ASCII code for f.i. character A is not 41H but 01H.
The 47-counter takes care of the horizontal and vertical positioning of the bits representing a character on the screen. These counters are each time before a character is displayed loaded with 47 (0010 1111).
When the memory location of the character which must be displayed is addressed the 47-counter starts counting down. The column of a selected character, addressed by the 3 most significant bits of the 47-counter, is applied on the output of the Character Generator.

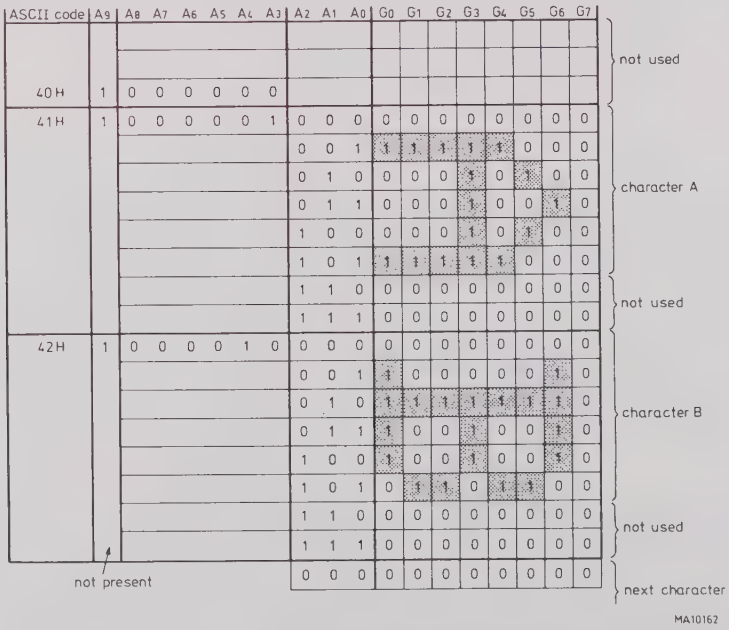


Fig.2.4 Character presentation

The bits of the column are scanned by the Column Scanner D2106 under control of the 3 least significant bits of counter D216. The output of Column Scanner D2016 is applied to OR-gate D2114. When the analyzer mode is selected the signal SWLZ is 0 so the level of the output (8) of OR gate D2114 depends on the output level applied by the Column Scanner D2106.
In oscilloscope mode SWLZ is 1 so the output of D2114 is, independent of the Column Scanner, a 1.

A 1 on the output (18) of D2114 causes an illuminated spot on the screen.
The three most significant outputs of the 47-counter also handle the horizontal positioning of the columns of a character on the screen. Therefore the digital output signal of the 47-counter is converted into an analog signal by a resistor network. (R1232, R1233 and R1234).

The 3 least significant bits of the 47-counter also handle the vertical positioning of the bits in a column. A resistor network (R1267, R1268 and R1269) is used for the digital to analog conversion.
When the 47-counter has counted down to 0000 0000 the outputs of the counter are set to 1111 1111 on the next positive going clock edge. On the positive going edge of the most significant output of D2108, output (5) of FF D2122, CHARDY, becomes a 1 and the inverted output (8) of FF D 2122 becomes a 0 by which the 47-counter is loaded again with (by 0010 1111).(i.e. 47 decimal).
When the logic scope is switched from scope to analyzer FF D2122 is set by SWLX.
When the logic scope is switched on FF D2122 is set by means of the signal $\overline{\text{RESET INT}}$ which also resets the microprocessor. If CHARDY is 1 (i.e. output 5 of FF F2122) the next character can be loaded, so the microprocessor makes $\overline{\text{LDCHAR}}$ a 0.
Output (3) of OR-gate D2114 becomes 0 and via $\overline{\text{ENASC}}$ the ASCII Latches are enabled and the Character Generator can be addressed via the data bus these lathces.
When the ASCII Latches are loaded and $\overline{\text{LDCHAR}}$ becomes 1, $\overline{\text{ENASC}}$ becomes 1 and on the positive going edge of this signal one-shot D2107 is activated. The negative pulse of 350 ns on the inverted output (12) resets FF D2122. The inverted output (8) of this FF becomes 1, which enables counting down the 47-counter.
While signal CHARDY is 1 the output (6) of OR-gate D2114 is 1 and no clock pulses are applied to the 47-counter.
After 350 ns output (5) of one-shot D2107 becomes 0. This negative going edge activates the 150 ns one-shot D2107.
The negative going edge on the inverted output (4) of this one-shot resets FF D2122. CHARDY becomes 0 and the 47-counter is counted down to 0000 0000 by clockpulses generated by te 2,4 MHz oscillator.
At this frequency the screen is diplayed 70 times per second. This oscillator runs as long as the analyzer mode is selected.
Before a character is displayed the electronbeam moves one position to the right, under control of the signal $\overline{\text{ENASC}}$.
When a number of blanks must be displayed, the microprocessor uses the "fast blank procedure" instead of the ASCII blank character. The microprocessor sets the fast blank signal in the ASCII Latch to 1 by which the one-shot is disabled and the 47-counter is prohibitted to count down so no characters are displayed.

The microprocessor moves the electronbeam to the right by means of the signal $\overline{\text{ENASC}}$.
The most significant bit of the data that is loaded in the ASCII Latches indicates if the character to be displayed must be intensified e.g. when the cursor is positioned on that character.

2.1.5.2. Character positioning

Before displaying a character the horizontal and vertical position have to be set.
Horizontally the display is devided in 43 positions and vertically in 64 positions.

Vertical deflection

The vertical position of the electronbeam on the screen is controlled by the microprocessor via the data bus lines D0...D5. When the control signal $\overline{\text{LDVERT}}$ is 0 the data present on the data bus is latched into Vertical Latch D2118.
The outputs of the Vertical Latch D2118 are connected to the 6 most significant inputs of the Vertical DAC D2117.
The inverted output (2) of the DAC shows a staircase deflection pattern.
The number of steps indicates the number of lines which are displayed on the CRT.
On this vertical deflection signal the signal VERT, which takes care of the vertical positioning of a bit in a character, is added. The "noise" on the staircase represents the signal VERT.
The deflection signal is inverted and amplified by operational amplifier D2121.
This analog signal is applied to the vertical amplifier of the oscilloscope.
The CRT starts writing at the top on the screen.
When the oscilloscope mode is switched on the signal YLSA becomes -12V so the differential amplifier circuit is made inactive and no vertical deflection signal is applied by the analyzer to the vertical aplifier of the oscilloscope.

2.1.5.3. Horizontal deflection

The horizontal position of the electronbeam on the CRT is determined by the counters D2102 and D2101.
The display is horizontally devided in 43 positions.
The counters start at 42 (0010 1010) and is counted down to 0 by control signal $\overline{\text{ENASC}}$. Each time a character is loaded in the ASCII Latches (D2111 and D2112) the counter decrements and the electronbeam moves to the right.
The horizontal positioning counters are loaded at the same time as the Vertical Latch, when $\overline{\text{LDVERT}}$ is 0.
The outputs of the counters are connected to the six most significant lines of DAC D2103.
The analog signal on the output of the DAC is inverted and amplified by opamp D2119. The output is a "staircase" signal.
This signal is applied to the horizontal amplifier of the oscilloscope.

The electronbeam starts at the left side on the screen.
The signal HORZ is added to the output of the horizontal DAC. This signal takes care of the column positioning in the character that is displayed.

2.1.6.Microprocessor, memories and decoders (See fig.7.7.)

2.1.6.1. Microprocessor

The whole scale of operations, from data acquisition to display, is controlled by the 8085 microprocessor D2324.

- The 8085 miroprocessor has a multiplexed address-data bus. The address lines A0...A7 are time-multiplexed with data lines D0...D7.
  Addresses and data are demultiplexed by Address Latch D2338.
  If the microprocessor sends out an address the signal ALE is a 1. The Address Latch latches the address on the falling edge of the ALE signal. After latching the least significant part of the address the AD bus becomes free for transport of data while the most significant address byte remains on the Address bus.
  Depending the level of the $\overline{RD}$ and the $\overline{WR}$ lines of the microprocessor data is written on or read from the addressed location.
- The 8085 is not garanteed to work until 500 usec after the supply voltage reaches 4,75V. during this period $\overline{RESET\ IN}$ is kept 0 by opamp D2343. When $\overline{RESET\ IN}$ becomes a 1 the microprocessor starts operating by fetching the first instruction from address 0000H. The microprocessor operates on a sequence of instructions stored in the EPROM's D 2337 A and B.
- Executing instructions the microprocessor can be forced to wait until peripheral device has ended its operation. The peripheral device sets the RDY input of the microprocessor to 0 when it is executing an operation. Every machine cycle the microprocessor examines the state of the RDY line.
  When the state of the RDY line is 0 the microprocessor is forced into a wait state preserving the exact state of the registers. The microprocessor completes its machine cycle when RDY has become a 1.
  A built-in option can force the microprocessor to wait until it has ended an operation by making OPTRDY a 0.
  The character display circuitry can force the microprocessor to a waite state by making CHARDY a 0. A2 and $\overline{DEC114}$ indicate if the character display circuitry is selected.
- Two interrupts of the microprocessor are used.
  When the interrupts are enabled and not masked out the microprocessor is interrupted and restarts operation at a specific memory address where a program is stored which handles this interrupt.
  A built-in option can interrupt the microprocessor via RST5,5 by making the signal OPTREQ a 1.
  The microprocessor can be interrupted via RST 6,5 by the signal DIRDY which indicates that data acquisition is stopped.
- The SID and the SOD take care of the serial in-and output of the contents of the accumulator. This facility is only used if the optional RS232C is built-in.

- The RESET OUT becomes a 1 after the microprocessor has been reset by $\overline{\text{RESET IN}}$. The RESET OUT signal is only used if options are built in.
- The microprocessor is forced in a hold state when the oscilloscope mode is selected to prevent noise produced by the microprocessor in operation. If the oscilloscope mode is selected the HLD input is made a 1.
  When the combi mode is selected the analyzer and the oscilloscope part must operate so HLD is made a 0.

2.1.6.2. Memories

The instructions the microprocessor needs to operate are stored in two EPROM´s D2337 A and B, size 4096x8-bits, addressed by address lines A0...A11.
The outputs of the EPROM´s are connected to the data bus.
The EPROM´s are selected by the control signals $\overline{\text{SROM1}}$ and $\overline{\text{SROM2}}$. The contents of these EPROM´s, the system software, is responsible for the sequence and nature of operations handled by the microprocessor.
RAM1 and RAM2 consist each of two 1024x4-bit RAM´s D2356 and D2376. The data in-and outputs of D2376 are connected to the data lines D0...D3; D2356 to data lines D4...D7. These RAM´s are enabled simultaneously by the control signal $\overline{\text{SRAM1}}$. The RAM´s can be written or read depending the status of the signal $\overline{\text{WR}}$ on the $\overline{\text{WE}}$ pin.
The selection of RAM2 is simular to the selection of RAM1. RAM1 and RAM2 are used by microprocessor for temporary storage of data e.g. reference data in the compare mode.

2.1.6.3. Decoders

The control and selection signals used in the analyzer cicuits are decoded out of the address lines A12...A15 by DECODER D2323, if the ALE and IO/$\overline{\text{M}}$ lines are a 0.

If ALE or IO/$\overline{\text{M}}$ are 1 the outputs of D2323 are all a 1. Some control signals are anded or ored which eachother or other address control lines to create in every situation the required control and selection signals.
DECODERS D2321 and D2311 decode address lines A0, A1 and A2 to control signals for reading the pushbuttons, writing the display and loading the Delay Counter. See memory map. Figure 2.5.

MEMORY MAP PM 3543			ADDRESS BUS														CONTROL BUS			DATA BUS								
		HEX	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	$\overline{WR}$	$\overline{RD}$	HEX	7	6	5	4	3	2	1	0	
$\overline{DEC\ 100}$	$\overline{SROM\ 1}$	0000 0FFF	0	0	0	0	x	x	x	x	x	x	x	x	x	x	x	x	1	0	xx	x	x	x	x	x	x	x	x	SELECT EPROM A (4K)
$\overline{DEC\ 101}$	$\overline{SROM\ 2}$	1000 1FFF	0	0	0	1	x	x	x	x	x	x	x	x	x	x	x	x	1	0	xx	x	x	x	x	x	x	x	x	SELECT EPROM B (4K)
$\overline{DEC\ 102}$	$\overline{SMEM\ 1}$	2000 2FFF	0	0	1	0	x	x	x	x	x	x	x	x	x	x	x	x	1	0	xx	x	x	x	x	x	x	x	x	SELECT MEMORY USED FOR OPTIONS
$\overline{DEC\ 103}$	$\overline{SMEM\ 2}$	3000 3FFF	0	0	1	1	x	x	x	x	x	x	x	x	x	x	x	x	1	0	xx	x	x	x	x	x	x	x	x	
$\overline{DEC\ 104}$	$\overline{SMEM\ 3}$	4000 4FFF	0	1	0	0	x	x	x	x	x	x	x	x	x	x	x	x	1	0	xx	x	x	x	x	x	x	x	x	
$\overline{DEC\ 105}$	$\overline{SMEM\ 4}$	5000 5FFF	0	1	0	1	x	x	x	x	x	x	x	x	x	x	x	x	1	0	xx	x	x	x	x	x	x	x	x	
$\overline{DEC\ 106}$	$\overline{SMEM\ 5}$	6000 6FFF	0	1	1	0	x	x	x	x	x	x	x	x	x	x	x	x	1	0	xx	x	x	x	x	x	x	x	x	
$\overline{DEC\ 107}$	$\overline{SRAM}$	7000 73FF	0	1	1	1	x	x	x	x	x	x	x	x	x	x	x	x	1/0	0/1	xx	x	x	x	x	x	x	x	x	A10=0→RAM1 (1K) A10=1→RAM2 (1K)
$\overline{DEC\ 108}$	$\overline{SDAMAP}$	8000 8FFF	1	0	0	0	x	x	x	x	x	x	x	x	x	x	x	x	1	0	xx	x	x	x	x	x	x	x	x	SELECT DATA-ACQUISITION MEMORY ADDRESS POINTER
			READING DATA ACQUISITION MEMORIES																($\overline{SDAM}$=0, $\overline{SDAMAC}$=0, $\overline{DAMIN}$=0)									
$\overline{DEC\ 109}$		9000 90FF	1	0	0	1	x	x	0	0	x	x	x	x	x	x	x	x	1	0	xx	x	x	x	x	x	x	x	x	READING PORT A PPI1
$\overline{DEC\ 109}$		9100 91FF	1	0	0	1	x	x	0	1	x	x	x	x	x	x	x	x	1	0	xx	x	x	x	x	x	x	x	x	READING PORT B PPI1
$\overline{DEC\ 109}$		9200 92FF	1	0	0	1	x	x	1	0	x	x	x	x	x	x	x	x	1	0	xx	x	x	x	x	x	x	x	x	READING PORT C PPI1
$\overline{DEC\ 109}$		9300	1	0	0	1	x	x	1	1	x	x	x	x	x	x	x	x	0	1	9B	1	0	0	1	1	0	1	1	CONTROLWORD INTO PPI1
			CLEARING THE DATA ACQUISITION MEMORIES																($\overline{SPPI1}$=0, $\overline{SDAMAC}$=0, $\overline{DAMIN}$=1)									
$\overline{DEC\ 111}$		B300 B3FF	1	0	1	1	x	x	1	1	x	x	x	x	x	x	x	x	0	1	80	1	0	0	0	0	0	0	0	SET CONTROLWORD INTO PPI1
$\overline{DEC\ 110}$		A000 A0FF	1	0	1	0	x	x	0	0	x	x	x	x	x	x	x	x	0	1	FF	1	1	1	1	1	1	1	1	WRITING DATA VIA PORT PA INTO DATA ACQUISITION MEMORIES
			WRITING THE TRIGGER WORD MEMORIES																($\overline{SPPI1}$=0, $\overline{STWM}$=0, $\overline{TWMWR}$=0)									
$\overline{DEC\ 111}$		B000	1	0	1	1	x	x	0	0	x	x	x	x	x	x	x	x	0	1	xx	x	x	x	x	x	x	x	x	WRITING PORT A
$\overline{DEC\ 111}$		B100	1	0	1	1	x	x	0	1	x	x	x	x	x	x	x	x	0	1	xx	x	x	x	x	x	x	x	x	WRITING PORT B
$\overline{DEC\ 111}$		B200	1	0	1	1	x	x	1	0	x	x	x	x	x	x	x	x	0	1	xx	x	x	x	x	x	x	x	x	WRITING PORT C
$\overline{DEC\ 111}$		B300	1	0	1	1	x	x	1	1	x	x	x	x	x	x	x	x	0	1	80	x	x	x	x	x	x	x	x	CONTROLWORD INTO PPI1
$\overline{DEC\ 112}$		C000	1	1	0	0	x	x	x	x	x	x	x	x	x	x	x	x	0	1	xx	x	x	x	x	x	x	x	x	WRITING THE TRIGGERWORD MEMORIES

Fig. 2.5 Memory map

MEMORY MAP PM 3543 (cont.)		ADDRESS BUS															CONTROL BUS			DATA BUS								
		HEX	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	$\overline{WR}$	$\overline{RD}$	HEX	7	6	5	4	3	2	1	0	
		SETTING THE CONTROL SIGNALS (SPPI 2 = 0)																											
$\overline{DEC\ 113}$	$\overline{SPPI2}$	D000	1	1	0	1	x	x	x	x	x	x	x	x	x	x	0	0	0	1	xx	x	x	x	x	x	x	x	x	WRITING PORT A
$\overline{DEC\ 113}$		D001	1	1	0	1	x	x	x	x	x	x	x	x	x	x	0	1	0	1	xx	x	x	x	x	x	x	x	x	WRITING PORT B
$\overline{DEC\ 113}$		D002	1	1	0	1	x	x	x	x	x	x	x	x	x	x	1	0	0	1	xx	x	x	x	x	x	x	x	x	WRITING PORT C
$\overline{DEC\ 113}$		D003	1	1	0	1	x	x	x	x	x	x	x	x	x	x	1	1	0	1	80	1	0	0	0	0	0	0	0	CONTROLWORD INTO PPI2
		READING THE SWITCHES																											
$\overline{DEC\ 114}$	$\overline{SCOL0}$	E004	1	1	1	0	x	x	x	x	x	x	x	x	x	x	1	0	1	0	xx	x	x	x	x	x	x	x	x	READ COLUMN 0
$\overline{DEC\ 114}$	$\overline{SCOL1}$	E005	1	1	1	0	x	x	x	x	x	x	x	x	x	x	1	0	1	1	xx	x	x	x	x	x	x	x	x	READ COLUMN 1
$\overline{DEC\ 114}$	$\overline{SCOL2}$	E006	1	1	1	0	x	x	x	x	x	x	x	x	x	x	1	1	0	1	xx	x	x	x	x	x	x	x	x	READ COLUMN 2
$\overline{DEC\ 114}$	$\overline{SCOL3}$	E007	1	1	1	0	x	x	x	x	x	x	x	x	x	x	1	1	1	1	xx	x	x	x	x	x	x	x	x	READ COLUMN 3
		WRITING THE DISPLAY($\overline{LDCHAR}$=0)																											
$\overline{DEC\ 114}$		E001	1	1	1	0	x	x	x	x	x	x	x	x	x	0	0	1	0	1	xx	x	x	x	x	x	x	x	x	LOADING A CHARACTER
		LOADING THE DELAY COUNTERS (LDDLYH=1, LDDLYL=1)																											
$\overline{DEC\ 114}$		E004	1	1	1	0	x	x	x	x	x	x	x	x	x	1	0	0	0	1	xx	x	x	x	x	x	x	x	x	LOADING THE MOST
$\overline{DEC\ 114}$		E005	1	1	1	0	x	x	x	x	x	x	x	x	x	1	0	1	0	1	xx	x	x	x	x	x	x	x	x	LOADING THE LEAST
		START DATA INPUT($\overline{STRDI}$=0)																											
$\overline{DEC\ 114}$		E006	1	1	1	0	x	x	x	x	x	x	x	x	x	1	1	0	0	1	xx	x	x	x	x	x	x	x	x	GENERATING A START PULSE
		TO OPTIONAL BOARDS																											
$\overline{DEC\ 115}$		Fxxx	1	1	1	1	x	x	x	x	x	x	x	x	x	x	x	x	0/1	1/0	xx	x	x	x	x	x	x	x	x	USED FOR OPTIONS

Fig. 2.5 Memory map

2.1.7. Pushbuttons interface (See Fig.7.7.)

The microprocessor must receive information from the user about the selected parameters. This information is fed from the pushbuttons via the data bus to the microprocessor.
During the execution of the program the microprocessor checkes repeatedly if the pushbuttons are manipulated.
The pushbuttons are addressed in a matrix via address lines A0, A1, A12, A13, A14 and A15.
The status of the pushbuttons is applied to the data bus if the active low control signal $\overline{SCOL}$ is 0.
This signal is controlled by DECODER D2321 which is selected if $\overline{DEC114}$ is 0 and RDB is a 1.
$\overline{DEC114}$ is a control signal decoded out of the address lines A15, A14, A13 and A12 DECODER D2323. $\overline{DEC114}$ is a 0 when the address lines A15, A14, A13 and A12 have the value 1110 (=14D). The microprocessor wants to read information from the pushbuttons so RDB is 1. The pushbuttons, addressed in a matrix, are devided over 4 columns, which are addressed by address lines A0 and A1 via DECODER D2321 (see figure 2.6. "Pushbutton matrix").
The active low column selection signals $\overline{SCOL0}$, $\overline{SCOL1}$, $\overline{SCOL2}$ and $\overline{SCOL3}$ are connected to the pushbuttons.
When a particular column is selected the information about the status of the pushbuttons, maximum 8, of that column is applied to DRIVER D2359, set on the data bus and applied to the microprocessor.
Each row of a column contains 1-bit of information about the status of a pushbutton. When a pushbutton of a column is pressed the active low $\overline{ROW}$ signal becomes a 0.
This information is inverted by the DRIVER, so a 1 on the data bus means that a pushbutton is pressed.
The logic scope checks if pod 2 is connected.
If the pod is connected $\overline{PODTST}$=0 so the output (6) of OR-gate D2349 becomes 0 when $\overline{SCOL1}$ is 0. The DRIVER sets the most significant data line to 1 and the microprocessor knows that pod2 is connected.
When pod2 is not connected the DRIVER makes the most significant data line a 0 and the microprocessor displays:
"POD2 NOT CONNECTED".
The threshold of the pod´s can be selected by switch S39.
The display time, in the AUTO mode, becomes 3,5 instead of 1 second when the pushbutton DISPT is pressed. Pressing it again resets the display time on 1 second.
The horizontal and vertical position of the displayed data on the screen can be adjusted by the potmeters R13 and R14. The intensity can be adjusted by potmeter R15.

Pushbuttons matrix

	$\overline{\text{SCOL 0}}$	$\overline{\text{SCOL 1}}$	$\overline{\text{SCOL 2}}$	$\overline{\text{SCOL 3}}$
$\overline{\text{ROW 0}}$	MENU	SEQ (DISPLAY)	LSA	0/DECR/BLANK
$\overline{\text{ROW 1}}$	TRIGW	SEQ (TRIGGER)	AUTO/ MAN	X/EXCH/INV
$\overline{\text{ROW 2}}$	DATA	DELAY	TRIG QUAL (EXT + WORD)	1/INCR/RCL
$\overline{\text{ROW 3}}$	-	FALSE	-	-
$\overline{\text{ROW 4}}$	COMP	GRAPH	DISPT	CURSOR RIGHT
$\overline{\text{ROW 5}}$	SPECL	option	option	CURSOR LEFT
$\overline{\text{ROW 6}}$	HEX	interface oscillos-cope	-	CURSOR DOWN
$\overline{\text{ROW 7}}$	EXCH	pod test PDTST	START/ STOP	CURSOR UP

Figure 2.6. Pushbutton matrix

2.2.DESCRIPTION OF THE OSCILLOSCOPE PART

2.2.1.General information

As the signal paths for channel A and channel B in the vertical deflection system are basically identical, only the channel B signal path is described.

2.2.2.Vertical deflection system

The vertical channels A and B are identical, each comprising an input coupling switch, an input step attenuator, an impedance converter and a preamplifier with trigger pick-off.
A channel multivibrator, controlled by the display mode pushbuttons, switches either channel A or channel B to the final Y amplifier via the dealy line driver and the delay line. The final Y amplifier feeds the Y deflection plates of the cathode-ray tube.
The individual stages of the vertical deflection system are now described in detail.

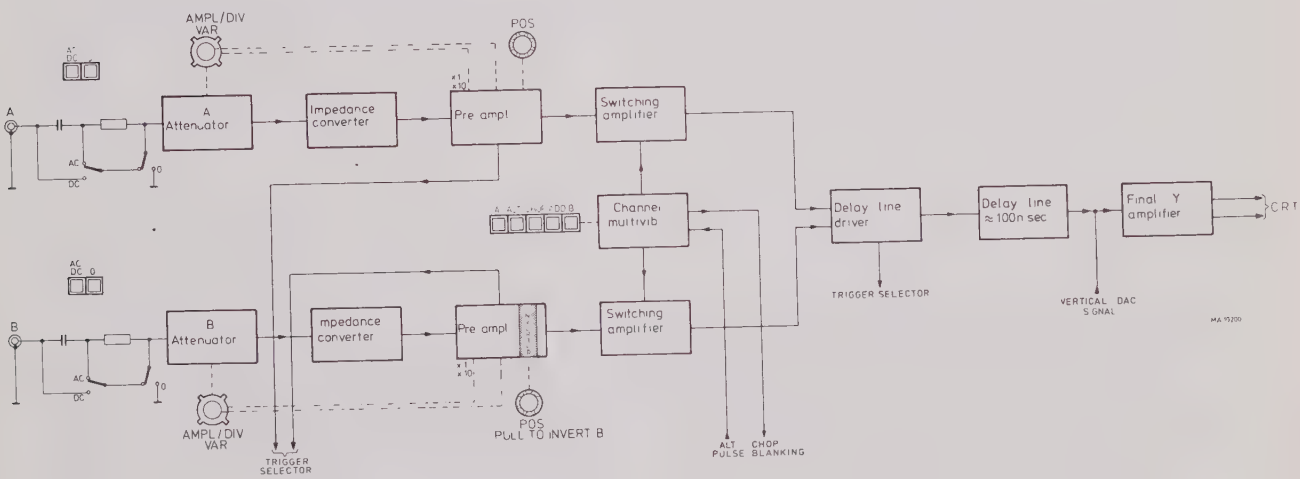


Fig.2.7 Vertical deflection system

2.2.2.1. Input coupling

Input signals connected to the B input socket X3 can be a.c. coupled, d.c. or internally disconnected. In the AC position of S14, there is a capacitor (C401) in the signal path. This capacitor prevents the DC component of the input signal from being applied to the amplifier.

In position DC of switch S14, the input signal is coupled directly to the step attenuator.
At the same time, blocking capacitor C401 is discharged via R402, to prevent damage of the circuit under test by a possible high charge.
S15 (0) isolates the B input signal and earths the channel input for reference purposes; e.g. for calibration or centering the trace.

2.2.2.2. Input attenuator

The input attenuator is a frequency-compensated, high-impedance voltage divider with twelve positions. The overall attenuation of the stage is determined by the combination of the selected sections of two voltage dividers. The various combinations are selected by the twelve positions of the frontpanel AMPL/DIV attenuator swithch S8.
The first divider sections attenuate by factor of 1.25, 3.125 and 6.25 and the second divider sections attenuate by a factor of 1x, 10x, and 100x.
With the overall combinations of attenuation, nine Y deflection coefficients are realised from 20 mV/div to 10 V/div in a 1-2-5 sequence. Only for the most sensitive positions 2 mV/div, 5 mV/div and 10 mV/div of AMPL/DIV attenuator switch S8, the gain of the Y amplifier is increased by a factor of 10.
The input capacitance of the attenuator cannot be adjusted in the individual positions. Small differences of approx. 1 pF are allowed.
The voltage divider sections are made independent of the input freqency range of the oscilloscope (i.e. 35 MHz) by means of the trimmers C407, C413, C416, C417, C418 and C419.

2.2.2.3. Impedance converter

The impedance converter is formed by V604 (two matched field-effect transistors). The two FET transistors are used in source follower configuration.
The signal level on the gate (and on the source) of the upper FET amounts to 1.6 mV/div or 16 mV/div.
Diode V601 together with the output impedance of the attenuator and also the attenuator action protects the input source follower, against excessive negative input signals. The d.c. balance of the circuit can be adjusted with R604, providing attenuator balance for the 10 mV/div and 20 mV/div positions.

2.2.2.4 Preamplifier

The input stage formed by D601 (5 transistors) is switched in a Cherry-Hooper configuration and direct coupling employed throughout.
In the positions 20 mV/div - 10 V/div of te AMPL/DIV switch S8, contact K601 is open and gain is determined by

$$\frac{R628 + R632}{R611 + R612} = \text{approx. } 1{,}8x$$

If K601 is closed (in positions 2 mV/div, 5 mV/div and 10 mV/div) the gain of this stage is increased by a factor of 10. This accurately adjusted with R621. To prevent jumping of the trace when K601 is switched with the input short circuited, no voltage must be present across these contacts. R604 (attenuator balance) serves this purpose.
R8 in conjunction with R622, R623, R624 and R626 forms the vernier control. In the calibrated position (R8 is 1 ohm) the transfer of this network is 0,85x. With R8 to its minimum position (o ohm) the transfer is 0,3x. Thus we have a control range of 3x.
V608, V609, V613, V616 and V617 form a symmetrical cascode circuit supplying an output CURRENT to the channel switch.
The tranfer conductance of this stage is:

$$\frac{I_{out}}{U_{in}} = \frac{1}{R641 \;//\; (R637 + R638) \;//\; (R646 + R647 + R648)} = 7 \text{ mA/V}$$

The signal level at the input of this stage is aprox. 24 mV/div equivalent to approx. 170 uA/div at the output.

Note: The channel A gain can be equalised to the channel B gain with the aid of R543 (gain x 1 in channel A amplifier).

2.2.2.5. Trigger pick-off

The trigger signal is picked-off at the emitters of V608 and V609, a signal source with a low internal resistance, by the series feed-back stage V611 and V612.
From this stage the trigger signal current is fed asymmetrically to the trigger selector via a 50 ohm cable.

Normal invert switch

The B channel has a provision for inverting the polarity of the Y signal. Push-pull switch S4, PULL TO INVERT B, is mounted on the shaft of front-panel control B POSITION. In the invert position of the switch the normal signal paths are blocked because V613 and V614 are switched off.
Inversion is achieved by V616 and V617 providing alternative paths for the signal when their bases are switched less positive by S4. Possible unbalance between the two positions of the switch can be compensated by preset potentiometer R647 (Norm invert balance).

Position control

Potentiometer R3 is the vertical POSITION control. Its balance is adjustable by means of R647 (shift balance).

Channel multivibrator

The channel multivibrator consists of two circuits which are inserted in the A and B channel signal paths.
The A channel circuit consists of the transistors V524, V526 and the diodes V521, V522 and V523. The B channel circuit consists of the transistors V624 and V626 and the diodes V621, V622 and V623. When the junction of the three diodes is positive in relation to mass, the diodes are non-conductive. The transistors, and thus, the signal path are conductive.
If the current drained from the junction exceeds 6 mA, the diodes are conductive and the transistors are turned off.The circuits are driven from the flip-flop formed by the transistors V703 and V704.

With A (S1) depressed: only channel A is displayed.
The base of V703 is connected to the -12 V supply voltage. V703 is turned-off then, its collector voltage is high and channel A is switched on. At the same moment channel B is switched off.

With ALT (S1) depressed: channels A and B are alternately displayed.
This push-button is a dummy and has no contacts, but it releases all the other

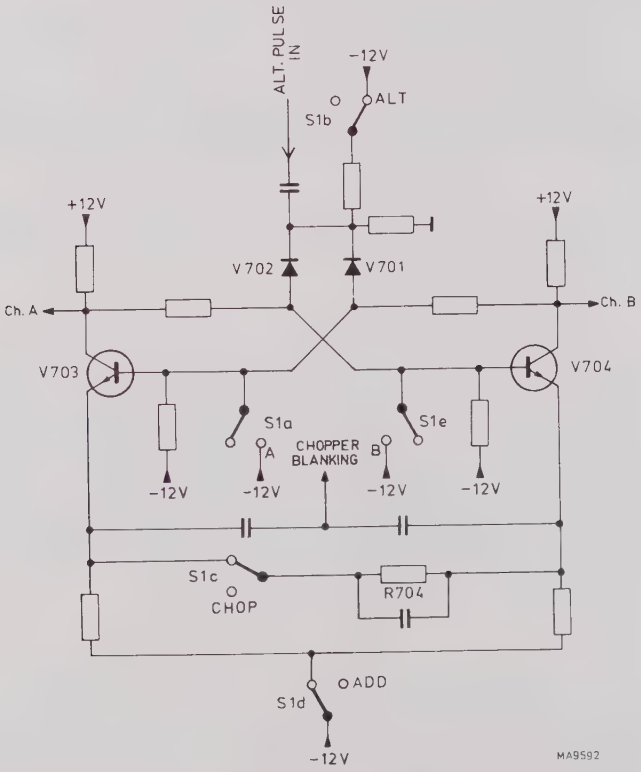


Fig. 2.8. Simplified diagram of the channel multivibrator.

push-buttons of the display-mode controls. In this mode there is a DC path via R704 between the two emitters, the circuit is bi-stable and one of the diodes is conductive.
V1201 is not conducting in ALT mode and negative going alternate pulses derived from the time-base generator are fed to the circuit. These pulses switch the circuit at the end of each sweep and the channels A and B are alternately displayed.

In the ALT mode -12 V is applied via S1 (A), S1 (CHOP), S1 (ADD) and S1 (B) and R710 to transistor V1506 in the beam blanking amplifier.
This transistor is then blocked and the only control signal for the beam unblanking amplifier is the normal unblanking pulse coming from the time-base circuit (D1203 via R1213).

With CHOP (S1) depressed: channels A and B are chopped.
In this mode the circuit acts as a chopper generator. S1 is open then, the DC path between the emitters of V703 and V704 is interrupted and the circuit is a-stable. Both diodes V701 and V702 are then turned-off and the circuit starts oscillating, the oscillating frequency being approx. 500 kHz.
During the switching transients in the CHOP mode, the c.r.t. is blanked with the aid of differentiated chopper blanking pulses (at the junction of R703 and C702) which are fed to the Z-amplifier.

With ADD (S1) depressed: channel A and B are added.
Both transistors are turned-off, both collector voltages are high and both channels are switched on.

With B(S1) depressed: only channel B is displayed.
The base of V704 is connected to the -12 V supply voltage. V704 is then turned-off, its collector voltage is high and channel B is switched on. At the same moment channel A is switched off.
In the LSA mode, generation of chopper is stopped by connecting a -12 V to the base of transistor V704.

Delay line driver

The symmetrical delay line is sandwiched between a series feed-back push-pull amplifier and a shunt feed-back push-pull amplifier, consisting of integrated circuit D801.
This amplifier combination is called "CHERRY-HOOPER" circuit.
The series feed-back stage receives a signal of approx. 30 mV/div which is obtained from a signal current of 0.17 mA/div from the channel switch, multiplied by the value of the load resistance R803 + R804 = 200 ohm.
The emitter impedance of the series feedback stage consists besides RE = R819 + R821 of the parallel circuit of a number of RC networks. As the delay line is a source of distortion for higher frequencies, these networks provide the necessary delay line compensation.
At the input side, delay line D802 terminates in R828 and R829 (totally 200 ohm).
The delay line itself is a symmetrically mounted spiralized cable with a characteristic impedance of 200 ohm and a delay of 110 nsec/m. At the output side, the cable terminates via R831 and R832 in the virtual earth points of the shunt feed-back stage. The input impedance on these virtual earth points is 14 ohm. This value in series with the 86.6 ohm of R831 and R832 forms the correct termination for the delay line. C814 and C816 are used for HF correction. The virtual earth points are also the points to which the output signals of the vertical D.A.C. are fed.
In the LSA mode the vertical channel is turned-off by applying a -12 V to the base of current source transistor D801 (12, 13, 14), in the series feed-back stage.

2.2.2.10 Composite trigger pick-off

The composite trigger signal is picked-off at the emitters of the series feed-bak stage (D801), an amplifier with a low emitter resistance, due to the series feed-back by V802 and V803. From the collector of V803 the composite trigger signal current is fed to the trigger selection switch (S16) via a 50 ohm cable.

2.2.2.11. Final Y amplifier

The output signals of the shunt feed-back stage are applied to the final Y amplifier stage consisting of the transistors V804, V806, V807 and V808, which are configured as two series feed-back amplifiers in parallel fed by a constant current source.
The gain of the final amplifier can be set by means of potentiometer R848. The centre taps of the coils L801 and L802 are connected to the Y deflection plates of the c.r.t. The Y deflection plates form filters together with the coils L801 and L802. These filters terminate in resistors R859, R861, R862 and R863.

2.2.3. Triggering

2.2.3.1. Trigger-source selection

The trigger source switches for triggering the time-base generator, can select any of the following input sources:
- an internal signal from the vertical A channel
- an internal signal from the vertical B channel
- an internal composite signal of channel A and channel B
- a signal derived from the analyzer circuit
- an external source
- an external source combined with a signal derived from the analyzer circuit.

All these sources can be used for both triggering and X deflection purposes. Source selection is done by means of a trigger selector switch S16 that feeds the trigger signals to the trigger circuitry.

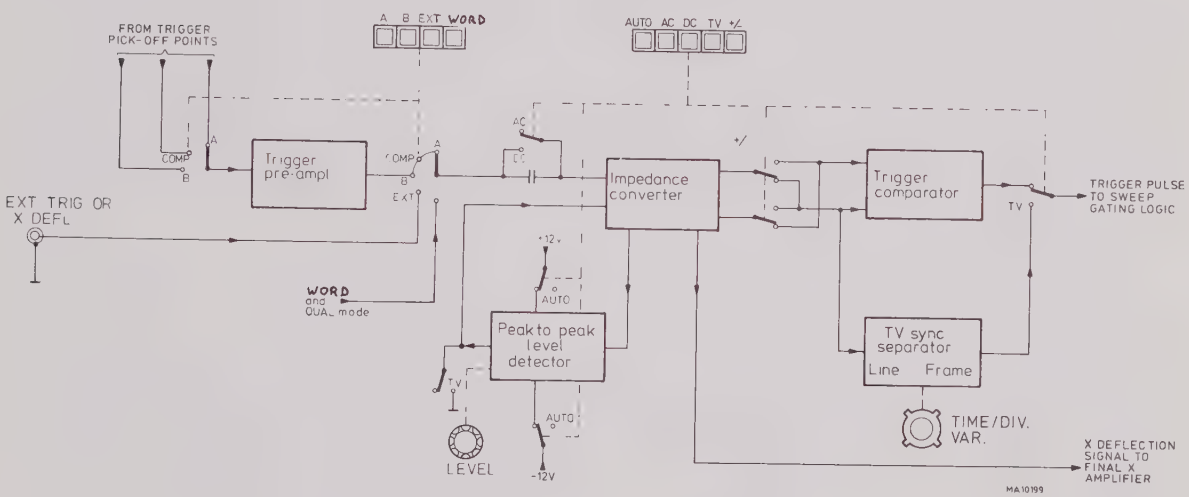


Fig.2.9. Trigger circuit

2.2.3.2. Trigger preamplifier

The signal currents (60 uA/div) of the three trigger pick-off stages (A, B and Comp) are, after selection by S16, amplified to a level of 100 mV/div by a shunt-feed-back stage + emitter follower stage consisting of V351 and V352. After this stage there is a selection between its output signal, a signal on the external socket and a signal which is derived from the analyzer circuit. Signals which are not used are short-circuited to mass.

2.2.3.3. Impedance converter

The trigger signal of 100 mV/div is fed via the AC-DC coupling switch S2 to a FET (V1006) in source follower configuration.
From here the signal is applied via an emitter follower to the ± slope selection switch (part of S2). This selection switch enables triggering on either the positive-going or the negative going edge of the triggering signal.

2.2.3.4. Trigger comparator

From the ± slope selector switch the signal is fed via a common emitter amplifier D 1001 (123/345) to the output shunt feed-back amplifier V 1014 via the TV mode switch (S2). The voltage gain is high (28x) but its dynamic range is small (2.8 Vp-p at the output). This is because of the tail current supplied by transistor D 1001 (12, 13, 14) of the symmetrical common emitter stage which is 2 mA. The current sweep at the output of this stage is consequently 1 mA at max. which is transformed into a 2.8 V max. voltage sweep at the output of the shunt feed-back amplifier V1014. This means that the trigger amplifier is completely driven at a trace height of 1 div. Which division on the screen this is, depends on the position of the LEVEL control R5. The trigger comparator is blocked in the analyzer mode by switching of the current transistor D 1001 (12, 13, 14). To this end minus 12V is applied to the base of this transistor.
With AC (S2) or DC (S2) depressed, the range of the LEVEL control is fixed. The DC voltage at the wiper of LEVEL control R5, which is fed to the FET (V1006) can vary between +3.5 V and -3.5 V. Diodes V1001 and V1002 are then turned off, and the voltage on the gate of the FET is then adjustable between +0.9 and -0.9 V. At a signal level on the gate of the other FET of 100 mV/div, there will be a control range of ± 9 div.

2.2.3.5. Peak to peak level detector

If the TV mode push-button (S2) is depressed, the LEVEL control is switched off. The wiper of R5 is then connected to mass. A synchronisation separator for the television signals is then inserted into the trigger signal path.

A composite video signal contains, besides the video information, also synchronisation pulses with line and frame frequency which can be distinguished by their pulse width.
The TV synchronisation separator circuit is able to:
1. separate the synchronisation pulses from the video information.
2. distinguish between frame synchronisation pulses and line synchronisation pulses.

The first requirement is met by V1013 acting as a DC restorer and limiter, the second requirement by the integrating network R1047, C1011 and C1012.
The TV signal is picked-off at the ± slope selector switch which in this case can be set for the right polarity of the RV signal. The TV trigger signal is

then amplified by the series feed-back push-pull stage V1009, V1011 and applied to synchronisation separator V1013 via emitter follower V1012. The signal on the base of V1013 could be as follows

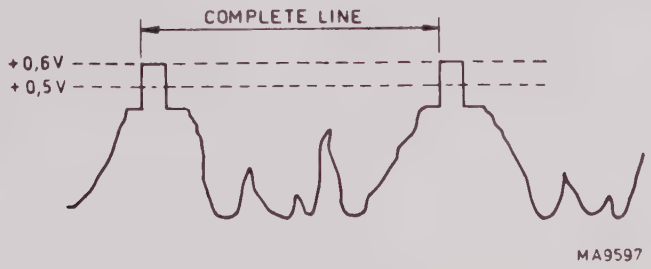


Fig. 2.10. Signal on the base of transistor V1013

The peaks of the synchronisation pulses are all held at one level by the DC restorer action of C1007, R1039 and the base emitter diode of V1013. The base voltage will never exceed +0.6 V by a large amount, but the complete waveform will appear at the base. The signal level is at this point approx. 280 mV per screen div. Change in signal of approx. 100 mV is sufficient to turn off V1013. V1013 looks only to the peaks of the synchronisation pulses.
The rest of the TV signal has no influence. On the collector of V1013 we find exclusively the synchronisation signal consisting of line synchronisation pulses and the wider frame synchronisation pulses.

In the time base positions 20 usec/div and faster, this complete signal is transmitted to the time base generator and we have line triggering. In the time base positions 50 usec/div. and slower, C1011 and C1012 are connected to mass. The narrower line synchronisation pulses are then integrated out of the signal, but the wider frame synchronisation pulses remain, and frame triggering is obtained. A second threshold is built-up by V1016. V1017 reacts to the signal that still passes and consists of pure line or frame synchronisation pulses. After this the signal is fed to the time base generator via V1014.

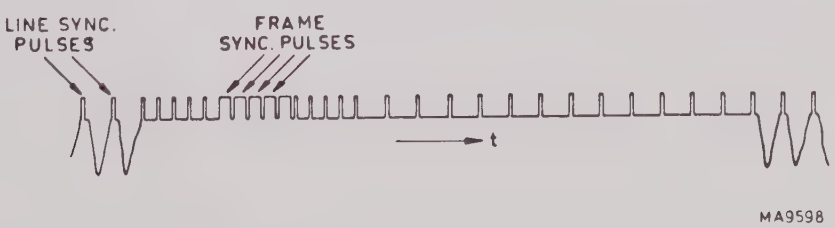


Fig. 2.11. A vertical interval with frame synchronisation pulse group

2.2.4. Time-base generator circuitry

2.2.4.1. Time-base generator

The time base generator comprises a sweep gating logic, a sweep generator, a hold off circuit, an auto sweep circuit and X final amplifier.

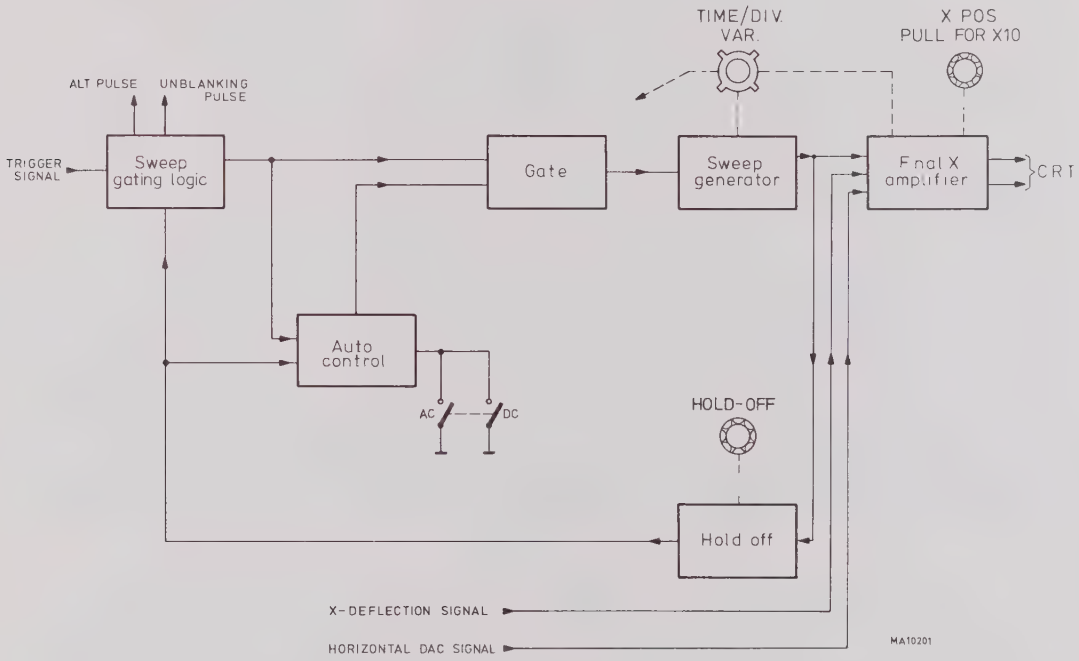


Fig. 2.12. Time-base generator

Before considering these stages in detail, the general principle is briefly described. Basically, the sweep gating logic, under the control of trigger signals from the trigger comparator and feedback pulses from the hold-of circuit, supplies square-wave pulses to the switching transistor V1213 of the sawtooth generator.
The time-base capacitors (effectively in parallel with the switching transistors) are charged linearly through a constant-current source to provide the forward sweep then are discharged rapidly by the switching transistor to provide the flyback period. The resulting sawtooth is fed to the X-final amplifier.

2.2.4.2. Sweep generator

The sweep speed or time coefficient is determined by the value of the time-base capacitance in circuit and by the magnitude of the charging resistor selected. The time-base capacitors are C1204 and C1207. Capacitor C1204 is always in circuit, C1207 is selected by the transistor V1216. This transistor operates as an electronic switch and is either fully cut off or fully-conducting. It is switched on by the application of a positive voltage to its base from the TIME/DIV switch S10.
According to the position of S10, this transistor V1216 switches in the capacitor C1207 in parallel with C1204. As mentioned, the sweep speed is also dependent upon the magnitude of the accurate constant-current supplied by transistor V1212. This current can be adjusted in steps by selecting the emitter resistance of V1212 by means of the TIME/DIV switch S10. Continuous control of the charging current can be effected by varying the base drive to V1212 with the continuous sweep control, TIME/DIV potentiometer R9. In the CAL position of this potentiometer, switch S11 closes and the charging current is solely determinded by the calibrated emitter resistance.
To compensate for the temperature coefficient of the transistor, the base voltage of V1212 is supplied via transistor V1214.
This also has the advantage of reducing the load on the TIME/DIV potentiometer R9.
This transistor, in turn, has its base controlled by preset potentiometer R1232 when TIME/DIV switch S10 is in one of the positions. 5 s/div.. .5 ms/div. This provides a fine adjustment for the timing circuit in the slower sweep speeds. In these positions the preset potentiometer R1232 provides an additional measure of control over the base voltage of V1212. In the positions the preset potentiometer R1232 provides an additional measure of control over the base voltage of V1212. In the positions of S10 when C1207 is not in circuit, the diode V1218 is blocked and the preset control R1232 is inoperative.

The discharge circuit for the capacitors C1204 and C1207 consists of resistor R1219 and transistor V1213. This switching transistor is driven by the sweep gating logic via a number of diodes. Diodes V1207 and V1208 form an AND-gate for positive logic;V1209 and V1211 adapt the level to control transistor V1213. The resulting sawtooth voltage is taken from two transistors V1219 and V1221 in a kind of Darlington pair configuration. The sawtooth voltage amplitude at this point is approx. 5 V, and is fed to the X-final amplifier. C1209 improves the transfer of faster sawtooth signals at the expense of the input impedance which need not to be that high then.

As can be seen in fig 2.12. is the sawtooth voltage generated from a signal coming from one of the sources A, B, COMPosite, EXTernal or WORD via the analyzerports.

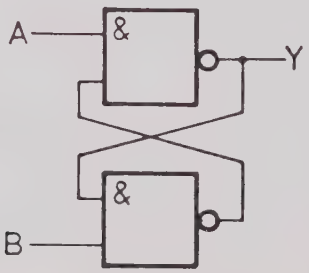
2.2.4.3. Hold-off circuit

The hold-off circuit prevents the sweep gating logic from responding to trigger pulses before the time-base capacitor has fully discharged. The sawtooth output from the Darlington pair V1219 and V1221 is applied to the base of emitter follower V1223. The switching transistor V1217 switches the hold-off capacitor C1208 in circuit, parallel to C1206, according to the position of the TIME/DIV switch S10, in a similar manner to that described for the time-base integrator timing capacitor. Capacitor C1206 is always in circuit irrespective of the TIME/DIV switch position. Charging current for the hold-off capacitors flows via transistor V1223. When V1223 cuts off the discharge current flows through R1228 and hold-off control R12. This current is adjustable to change the hold-off time. The voltage across hold-off capacitors C1206 or C1206 + C1208 follows the sawtooth voltage fairly fast in positive going direction via emitter follower V1223. When a certain value is reached, integrated Schmitt trigger D1201 reacts and the end of the sweep is initiated.
This is followed by a hold-off period in which the voltage across the hold-off capacitor decreases fairly slowly until the lower switching level of the Schmitt trigger is reached. The system can now be triggered again. In the meantime also the time-base integrator timing capacitor C1204 or C1204 + C1207 has reached its quiescent state. The output (point 6) of D1201 is low during the hold-off time, at any other moment this output is high.

2.2.4.4. Sweep gating logic

The sweep gating logic which consists of TTL logic circuit is controlled by the following signals:
- The trigger signals supplied by the trigger comparator.
- The voltage supplied by the hold-off circuit.
- The voltage supplied by the auto circuit via the hold-off circuit.

The TTL circuit D1201 contains four 2-input NAND-gates with Schmitt-trigger properties. D1201 contains four normal 2-input NAND-gates and D1203 contains three normal 3-input NAND-gates. With the aid of the various gates two flip-flops are formed.



A	B	Y
0	0	1
0	1	1
1	0	0
1	1	Old situation

MA9599

Fig. 2.13. Sweep gating logic signals.

Y is A, if B is 0
Y is 1, if A is 0

The circuit is set by A is 0 (when B is 1) and reset by B=0 (when A is 1). See relation diagram of the sweep gating logic in the AC or DC mode.

1 The incoming trigger signal from the trigger comparator switches the Schmitt-trigger output (D1201, point 11) to zero after a positive going edge has exceeded the upper switching level (+ 1.7 V) of this Schmitt-trigger.

2 After this, the first flip-flop output (D1202, point 3) is set to the logic 1-state.

3 If the negative going edge of the incoming trigger signal drops below the lower switching level (D1201 point 11) switches to logic 1 level again.

4, 5, 6 The logic 1 state of the first flip-flop and the output signal of the Schmitt-trigger allows the setting of the second flip-flop output (D1203 point 6) to the zero state by means of the NAND output (D1202 point 11).

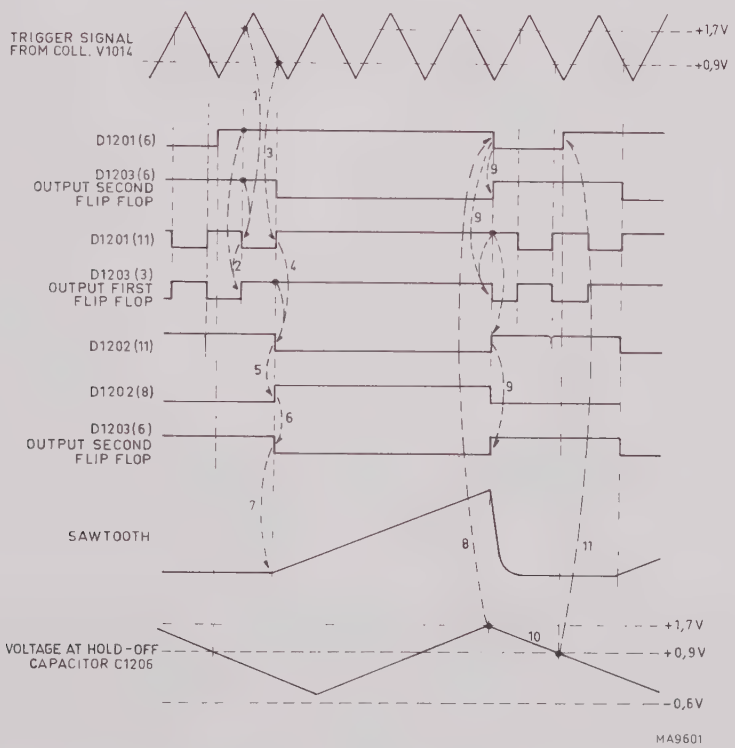


Fig. 2.14. Time relation diagram of the sweep-gating logic in the AC or DC mode

7 The output signal of the second flip-flop is applied to switching transistor V1213 via an OR-gate which consists of E1216, V1207 and V1208. This signal causes the sweep to start.

8 The end of the sweep is reached when the signal across the hold-off capacitor C1206 exceeds the upper switching level (+ 1.7 V) of the hold-off Schmitt-trigger. The output of this Schmitt-trigger switches then to zero.

9 Both flip-flops are now reset. Switching transistor V1213 starts conducting and time-base capacitor C1204 will discharge.

10 The voltage across the hold-off capacitor C1206 decreases slowly until the lower switching level (+ 0.9 V) of the Schmitt-trigger is reached.

11 This is the end of the hold-off period. The output (D1201, point 6) of the hold-off Schmitt-trigger rises to 1 again and the system can be triggered again.

2.2.4.5. Auto sweep circuit

In the absence of a trigger signal the auto sweep circuit will provide a display on the screen. Transistor V1203 senses the state of the output of the second flip-flop, this is the output of the sweep gating logic. When this point reaches the logic zero level, transistor V1203 starts conducting enabling C1202 to discharge. Transistors V1204 and V1206 are then turned off. The collector of V1206 lies on -0.7 V potential and the relevant gate of D1201 is then blocked. This means that output D1201 (3) is at logic 1 level (+5 V).
In the absence of a trigger signal, the output D1203 (6) of the sweep gating logic remains a logic 1 level (+5 V) and transistor V1203 remains turned-off. The voltage across capacitor C1202 increases until approximately 100 msec., transistor V1204 starts conducting and causes transistor V1206 to conduct. The collector of V1206 rises to approximately +5 V and the relevant gate of D1201 opens. The hold-off signal on point 6 of D1201 now can reach via gate D1201 (3) and the OR-gate, the switching transistor V1213. The loop is then closed and the time base generator is in the free running mode.

2.2.4.6. X-final amplifier

Transistor V1407 is driven by either the time-base generator via diodes V1411 and V1409 when R1406 is kept at +12 V level via TIME/DIV switch S10 (in all the TIME/DIV positions of this switch) or the amplifier stage V1404 when R1407 is kept at +12V level via TIME/DIV switch S10 (in position X DEFL), or the horizontal DAC via output socket X2101, when the analyzer mode is selected. Transistor V1404 receives its input signal from D1001 point 8 of the trigger amplifier. This signal is derived from one of the two amplifier stages in parallel (one for each deflection plate). Only one half is described.
The actual amplifier is the cascode circuit with transistors V1414 and V1416. The resistors R1428 and R1429 are feedback resistors.

The base current for the amplifier is supplied by transistor V1413. The average voltage on the deflection plate is kept at +26 V by means of zener diodes V1424 and V1426. Capacitor C1413 improves the h.f. response.
This final stage is supplied from the +180 V and -180 V because the X plates of the C.R.T. are mechanically displaced such that they are less sensitive than the Y plates.
The cascode amplifier stages are controlled via the transistors V1406 and V1407.

2.2.5. Cathode-ray tube circuit

The cathode-ray tube circuit comprises the C.R.T. itself and the brightness, focus, astigmatism, geometry and trace rotation controls and the beam blanking amplifier. A block diagram of the C.R.T. circuit is given in Fig. 2.15.

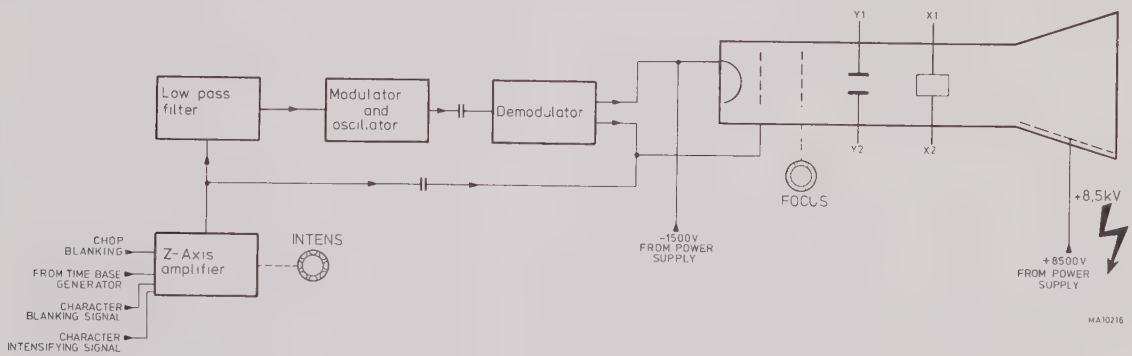


Fig. 2.15. Cathode-ray tube circuitry

2.2.5.1. C.R.T. controls

By means of the INTENS potentiometer R1, the brightness of the timing display can be continuously controlled. The display can be focused by means of the FOCUS potentiometer R6. Both INTENS and FOCUS controls are front panel controls.
The C.R.T. circuitry also has preset potentiometers for trace rotation, astigmatism and geometry.
The FOCUS control R6 forms a part of a voltage diviser network across the 1.5 kV output of the power supply. The slider of this potentiometer is connected direct to the focus, grid G3.

TRACE ROTATION is achieved by means of the trace rotation coil L1501. This coil mounted inside the mu-metal screen, provides a magnetic field for rotational control of the entire scan. The degree and direction of rotation is determined by the setting of front panel potentiometer R10 (screwdriver operated).

The slider of R10 is connected to the bases of the complementary transistors V1521 and V1522.

OPTIMUM

With the ASTIGMATISM control R1543, the form of the spot can be corrected by adjusting the voltage on the grids G2 and G4.

OPTIMUM

With the GEOMETRY control R1549 the barrel and pin-cushion distortion is corrected by adjusting the voltage on the grid G7.

OPTIMUM

MAT 104

2.2.5.2. Beam blanking amplifier

The beam blanking amplifier receives various input signals. One is a signal, originated in the time-base generator and is applied to the amplifier to unblank the trace during the sweep.Signals are supplied by the channel switch to blank the trace during switching from channel to channel in the chop mode and during the fly-back period of the sweep.
One is a character intensifying signal and is delivered by the ASCII latch D2111 in the interface oscilloscope and from the same circuit a character blanking signal is delivered. The INTENS potentiometer R1 determines the amount of input current fed to the amplifier.

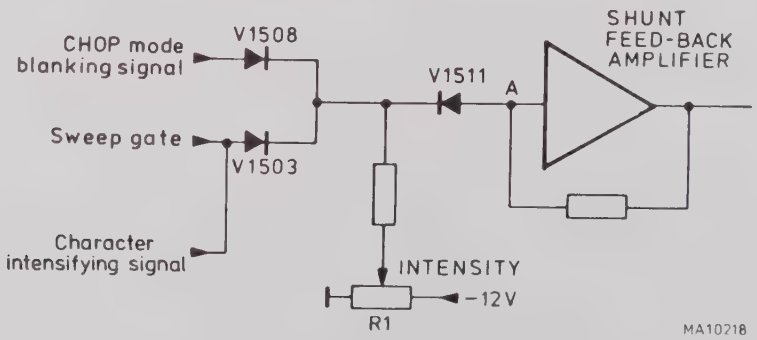


Fig. 2.16. Shunt feed-back amplifier.

In all the time/div. positions of the TIME/DIV switch S10, the anode of diode V1202 is kept at approx. +12 V, resulting in a logic 1 level at input 1 of NAND D1203.
The output point 12 of this NAND is now at logic 1 level when either input 1 or input 3 is low. In other words only during a sweep.

In the X DEFL position of the TIME/DIV switch S10, input 1 of NAND D1203 is at a logic 0 level, and in that case the output point 12 of this NAND is steady at logic 1 level. This output signal is inverted by a NAND and fed via diodes V1501 and V1503 of the beam blanking amplifier.
The chop mode blanking signal from the channel switch is fed to transistor V1506 via R1502. The inverted and amplified signal is applied to diode V1508. Both signals are joined together at the base of transistor V1514 (point A in figure 2.16. This is the virtual earth point of a shunt feed-back amplifier. Assume that V1503 and V1508 are turned-off by applying a logic zero to both inputs.
Then the output voltage of the amplifier can be varied with the aid of INTENS potentiometer R1. The light on the screen is variable then e.g. during a sweep or in the X deflection mode. A logic 1 on either one or both inputs of the diodes V1503 and V1508 turns V1511 off. The C.R.T. is then blank e.g. between sweeps or during the sweep when there is channel switching in the chop mode.

The blanking signal is amplified in the stage with transistors V1512, V1513 and V1514. At the output of this amplifier the a.c. and d.c. components of the blanking signal are guided along different paths. The a.c. path runs straight to the Wehnelt cylinder of the C.R.T. via capacitor C1512.
A d.c. signal is fed to the emitter of transistor V1517 via a low-pass filter R1528/C1508/R1527. Transistor V1517 constitutes a multivibrator together with transistor V1516. The a.c. voltage on the collector of V1517 has a peak-to-peak value which depends on the voltage fed to the emitter of V1516 by the shunt feed-back amplifier.

The a.c. voltage supplied by multivibrator V1516/V1517 is applied to a peak detector. This peak detector rectifies this a.c. voltage.

The reason for the a.c. and d.c. paths is to isolate the cathode and Whenelt cylinder, which are on a -1.5 kV potential, from the other circuits. The a.c. component of the blanking signal is transmitted directly to the high-voltage part via blocking capacitor C1512, which is a high voltage capacitor. The d.c. signal, however, is converted into an a.c. voltage and then transmitted to the high-voltage part, via capacitor C1509, after which it is rectified by means of diode V1519.
The dark level can be adjusted with the aid of potentiometer R1534 in the emitter circuit of transistor V1517 in the d.c. amplifier.

2.2.6. Power supply circuitry

The power supply comprises a mains transformer and rectifier, a DC to AC regulator and a transformer and output voltage rectifier.
The power supply also incorporates a circuit for the graticule illumination.

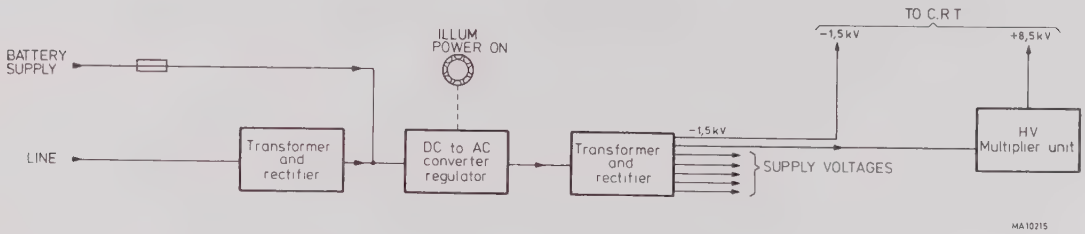


fig. 2.17. Power supply

The line part of these instruments power supply is double insulated and meets IEC 348 SAFETY CLASS II recommendations for metal-encased electrical equipment. This eliminates the need for a 3-wire power cord with earth connection.
The converter together with the primary of the converter transformer is electrically floating in relation to mass.
Therefore also the 24 V d.c. supply is floating.

2.2.6.1. Mains transformer

An incoming mains voltage is fed via the thermal fuse (F101) and the voltage selector S18 to the appropriate primary taps on the mains transformer T101. Transformer T101 has three primary windings which can be combined by means of voltage adapter S18. This combination allows the instrument to be used with mains voltages of 110 V, 127 V, 220 V and 240 V.

The voltage on the secondary windings of the transformer is full-wave rectified. The resulting negative d.c. voltage (approx. 24 V) across electrolytic capacitor C203, or alternatively a negative d.c. voltage on the rear panel DC POWER IN input socket X7, is applied to the voltage stabilizer and converter.

2.2.6.2. Converter and stabilizer

The converter is a square-wave generator operating at a frequency of approx. 18 kHz and driven by the d.c. voltage across the electrolytic capacitor C203.
A basic diagram of the converter is shown in Fig. 2.18.
In the converter, transistors V217′ and V217" function as switches and regulators and alternately connect the negative supply voltage to either end of the primary of T201/T202.

Assume that transistor V217′ has a slightly higher current gain than V217", then the positive voltage from the feed-back winding quickly drives transistor V217′ into saturation. The current in the top half of the primary of T201/T202 increases linearly at a rate determined by the inductance of the primary. This current increase continues until the iron in transformer coil T201 is saturated. Then the magnetic lines of flux stop changing and consequently no voltage is induced in the feedback winding. When its base drive creases, the transistor is cut off.
This reverses the polarity of the feedback voltage and transistor V217" is turned hard on. The bottom half of the primary then passes on increasing current until the core is saturated in the opposite direction.
The subsequent absence of feedback voltage inititates the switching back to V217′ and the cycle starts again.

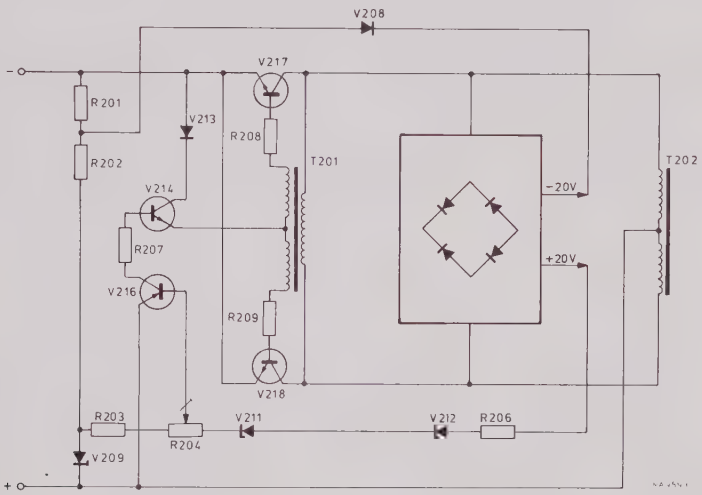


Fig. 2.18. Basic diagram of the converter

The regulation works as follows. When an input voltage is applied to the converter, the negative voltage across Zener diode V209 turns transistor V216 fully on, as there is no positive voltage from temperature compensation stabistors V211 and V212.
Then a base current flows via transistor V216 through resistor R207, through the base-emitter junction of transistor V214 (operating as a diode since diode V213 interrupts the collector circuit) and from base to emitter of both transisitors V217′ and V217".

As there is then an a.c. voltage across the primary of T201/T202, diodes V222 and V223 produce a positive d.c. voltage of +20 V across capacitor C209. This voltage reduces the current through transistors V216 and V214 sufficiently to limit the drive to transistors V217′ and V217" and produce the desired output level. The setting of potentiometer R204 determines the value of the regulated output voltage.

Possible differences from the set output voltage are fed back via the temperature compensation stabistors V211 and V212 to transistor V216 so that the drive of transistors V217′ and V217" is adapted so as to compensate for the differences. This also applies to mains voltage fluctuations.

After rectifying and smoothing, the secondary voltages +5 V, -5 V, +12 V, -12 V, +38 V, +180 V, -180 V, -1500 V and post accelaration voltage +8500 V are obtained. The voltage quintupler which supplies the +8500 V cannot be repaired and must be replaced when it breaks down.
T202 contains a separate secondary winding for the heater voltage for the C.R.T.
All supply voltages except the +8500 V and the -1500 V can be continuously short-circuited without damage to the components. Resistor R202 limits the collector current when the output is short-circuited and the switching action is stopped, thereby holding the dissipated power in transistors V217′ and V217" at a safe level. Thus, the power supply of the oscilloscope is fully protected against short-circuits. A short-circuit is indicated either by a squeaking noise coming from the power supply or by the pilot lamp B1, which indicates the ON state of the oscilloscope, failing to light up.
If supplied by an external d.c. voltage, the instrument is protected against overloads and wrong polarity by internal fuse F201 and diode V206.

2.2.6.3. Illumination circuit

The graticule of the C.R.T. can be illuminated by means of the bulbs E1. The intensity can be varied with the aid of ILLUM potentiometer R11 which controls the collector current (which is current through the bulbs) of transistor V207. The illumination circuit is not short-circuit proof.

2.2.7. Calibration circuit

The calibrator circuit consists of transistors V1602 and V1603, which are configured as a stable multivibrator such as used in the channel switch. Good shape of the wave-form is obtained by a constant current supplied by transistor V1602 which will flow in turn through the left hand or right hand transistor. The amplitude is 1,2 V or 6 div in the 20 mV/div attenuator positions. (The straight through position of the attenuator.) Potentiometer R1607 allows accurate adjustment of the amplitude of the calibrator output voltage. This square-wave output voltage is taken from the collector of transistor V1603 and fed to socket X1. This is the front panel CAL terminal. The calibrator output signal can be used for probe compensation and/or checking the vertical deflection accuracy.

3. CHECKING AND ADJUSTING

3.1. General information

The following information provides the complete checking and adjusting procedure for the PM3543 and PM 3542 logic-scopes. As some of the circuits are interdependent, the given order of checking is advised. The procedures are, therefore, presented in a sequence that is best suited to this order. Prior to checking and adjusting a particular circuit, care must be taken to ensure the accuracy of all associated circuits.

3.1.1. Safety regulations (in accordance with IEC 348)

Before connecting the instrument to the mains (line), visually check the cabinet, controls and connectors, etc. to ascertain whether any damage has occured in transit. If any defects are apparent, do not connect the instrument to the mains (line).

The instrument must be disconnected from all voltage sources, and any high voltage points discharged before any maintenance or repair work is carried out. If adjustments or maintenance of the operating instrument with covers removed is inevitable, it must be carried out only by a skilled person who is aware of the hazards involved. In normal operation the double-insulated power supply obviates the need of a safety ground. Bear in mind that the capacitors inside the instrument may still be charged even if the instrument has been separated from all voltage sources.Never remove a cicuit board until the instrument has been switched off for at least one minute.When an instrument is brought from a cold to a warm environment, condensation must cause a hazardous condition. In this situation, you must allow approximately 30 minutes (i.e. recovery time, see 1.3.3. "Environmental characteristics") for your logic-scope to acclimatize until all condensation has evaporated.

Warning :	It must be borne in mind that in all measurements the frame ground of the instrument is raised to the same potential as that of the measuring ground probe connections. Neither the probe´s ground lead nor the frame ground shall be connected to live potentials.

The tolerances stated in the checking and adjusting procedures apply only to instruments which are completely set up, and may differ from the data given in the specification chapter i.e. 1.3. CHARACTERISTICS.
All adjusting elements have been listed in the headings of the various sections. Allow a warming-up time of 30 minutes before checking and adjusting.

3.2. Test equipment and tools required

For a complete checking and adjusting procedure, you will need the tools and test equipment listed in the following table.

TEST EQUIPMENT

Description of test instrument	Specification of the test instrument	Suitable test instrument	Usage
Digital multimeter	AC/DC instrument accuracy within 0,1%	Philips PM 2526 or equivalent	C.R.T. circuit Trouble
Timemark generator.	Providing markers of 0,55 to 0,1 us, accuracy within 0,5%	-	Time-base timing checks.
T.V. patern generator or T.V. source	Providing frame and line sync pulse output. Ampl. at least 40 mV.	Philips PM 5519 or equivalent.	Time-base, T.V. triggering.
Squarewave generator or amplitude calibrator.	Providing output voltages variable from 10 mV to 12 V (accuracy within 0,5%), frequency range 2 KHz...1MHz, rise time $\leq$ 3 ns.	-	Attenuator response, vertical gain and response checks.
Sinewave generator.	Providing output voltages variable from 10 mV to 10 V frequency range 20 Hz...35MHz.	Philips PM 5167 suitable for most purposes.	Vertical amplibandwidth and triggering checks. Trouble shooting.
Monitor oscilloscope and analyzer or combination.	0...35 MHz bandwidth	Philips PM 3543 or equivalent.	Trouble shooting Adjusting.
Or monitor oscilloscope	4 channels, 100 MHz	PM 3264	Trouble shooting Adjusting.

Pulse generator	1Hz ... 50 MHZ Rise and fall time $\leqslant$ 4 nsec.	Philips PM 5712	Adjusting
Amp.-meter.	Moving-iron meter.	-	Mains current consumption.
Variable mains transformer.	Well insulated for safe checking.	Philips 2422 529 00005.	Trouble shooting
Probe 10x attenuation.	Suitable for input capacities of 20 pF to 30 pF.	Philips PM 8925 or equivalent.	Trouble shooting
Logic pulser.	Provides in-circuit stimulus.	See Fig. 4.3.	Trouble shooting
Logic tracer.	To indicate the in-circuit stimulus.	See Fig. 4.3.	Trouble shooting
Trimming tool kit.	Low capacitance trimming tool.	Philips	Adjusting and maintenance.

3.3. Power supply

3.3.1. Mains current

- Check that the mains voltage adapter (S18) has been set to the local mains voltage and connect the instrument to such a voltage.
- Switch the oscilloscope on and check that the pilot lamp on the front panel lights up.
- Check that the current consumption does not exceed 60 W local when no options are built-in and 64 W at local mains when the options are built-in (Measured with a moving iron meter).

3.3.2. Supply voltages (R204)

- Check that the voltage across capacitor C224 is +12 V, + or -0,25; if necessary readjust potentiometer R204 (Fig. 3.1).
- Check the supply voltages in accordance with the following table:

voltage across	Required value	Max. allowable ripple
C227 (Fig. 3.1.)	+ 5 V, ±0,2 V	⩽ 2 mVp-p
C224 (Fig. 3.1.)	+ 12 V, ±0,25 V	⩽ 4 mVp-p
C229 (Fig. 3.1.)	- 12 V, ±0,25 V	⩽ 4 mVp-p
C222 (Fig. 3.1.)	+ 38 V, ±2 V	⩽ 40 Vp-p
C231 (Fig. 3.1.)	-180 V, ±9 V	⩽ 1 Vp-p
C221 (Fig. 3.1.)	+180 V, ±9 V	⩽ 1 Vp-p
C211 (Fig. 3.1.)	6,3 V, ±0,6 V	.....

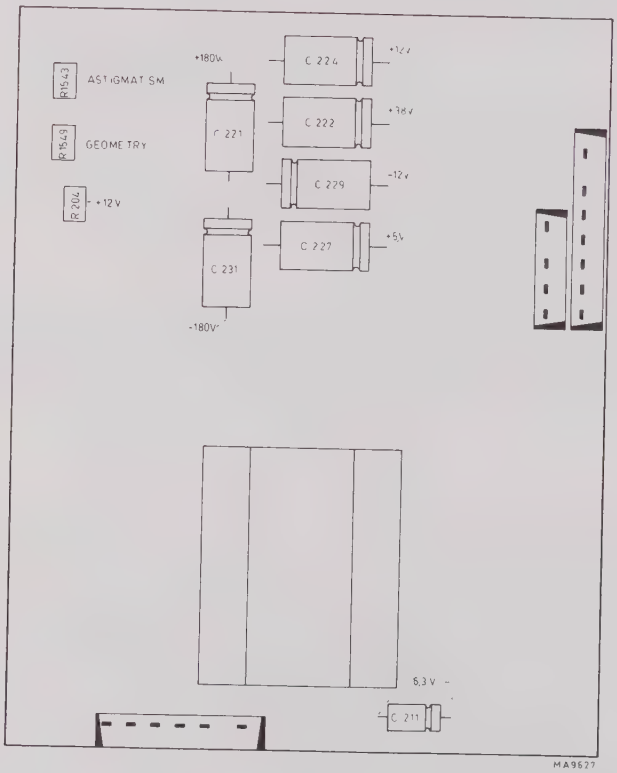


Fig. 3.1. Adjusting and checking the power supply.

- Vary the a.c. voltage to which the instrument is connected + or -10% of the nominal voltage.
- Check that the supply voltages do not vary more than + 2% and tat the ripple voltages do not exceed the values mentioned in the table above.

3.4. Oscilloscope section

3.4.1. Cathode-ray tube circuit

3.4.1.1. Brilliance (R1534)

- Depress push-button A of the display mode switch S1.
- Set TIME/DIV switch S10 to position EXT X DEFL.
- Depress push-button EXT of the trigger source selector switch S16.
- Set A POSITION potentiometer R2 and X POSITION potentiometer R4 to their mid-positions.
- Set INTENS potentiometer R1 to 90° from its left hand stop.
- Adjust potentiometer R1534 (Fig 3.3.) until spot just disappears.

3.4.1.2. Trace rotation (R10)

- Depress push-button AUTO of the trigger mode switch S2.
- Set TIME/DIV switch S10 to 0,1 ms/div.
- Depress push-button A of the display mode switch S1.
- Depress push-button A of the trigger source selector switch S16.
- Depress the input coupling switch S13 (0).
- Center the time-base line using A POSITION potentiometer R1.
- Check that the time-base line runs exactly in parallel with the horizontal lines of the graticule. If necessary, readjust front panel TRACE ROTATION potentiometer R10.

3.4.1.3. Focus and astigmatism (R1543)

- Depress push-button A of the display mode switch S1.
- Depress push-button A of the trigger source selector switch S16.
- Depress the input coupling switch S12 (AC).
- Release the input coupling switch S13 (0).
- Set A AMPL/DIV switch S6 to 0,1 V/div and A AMPL/DIV potentiometer R7 to CAL
- Set TIME/DIV switch S10 to 50 µs/div and TIME/DIV potentiometer R9 to CAL.
- Apply a sine-wave voltage of approx. 600 m Vp-p, 10 kHz, to the A input socket X2.
- Set INTENS potentiometer R1 for normal brightness.

Use an insulated screw-driver.

- Adjust FOCUS potentiometer R6 and astigmatism potentiometer R1543 for a sharp and well-defined trace (Fig. 3.1).

3.4.1.4. Geometry (R1549)

- Set the controls as in the previous section.
- Set A AMPL/DIV switch S6 to 5 mV/div and A AMPL/DIV potentiometer R7 to CAL.
- Apply a sine-wave voltage of approx. 600 mVp-p, 10 kHz, to the A input socket X2.

Use an insulated screwdriver

- Check that the displayed vertical lines are as straight as possible. If necessary readjust potentiometer R1549 (Fig. 3.1.).

3.4.2. Y-amplifier balance

3.4.2.1. General information

The adjustments of the vertical amplifier channels A and B are identical. The knobs, sockets and adjusting elements of channel B are shown in brackets after those of channel A.

3.4.2.2. D.C. balance (R504, R604)

- Depress push-button A (B) of the display mode switch S1.
- Depress push-button AUTO of the trigger mode switch S2.
- Depress the input coupling switch S13 (S15) (0).
- Set AMPL/DIV potentiometer R7 (R8) to CAL.
- Centre the trace using A (B) POSITION potentiometer R2 (R3).
- Check that the trace does not jump if AMPL/DIV switch S6 (S8) is switched from 10 mV/div to 20 mV/div. If necessary, adjust potentiometer R504 (R604) for minimum jumps (Fig. 3.3.).
- Repeat the measurement for channel B.

3.4.2.3. Gain balance (R514, R614)

- Depress push-button A (B) of the display mode switch S1.
- Depress the input coupling switch S13 (S15) 0.
- Check that the trace does not move when the AMPL/DIV potentiometer R7 (R8) is rotated. If necessary readjust R514 (R614) (Fig. 3.3.).
- Repeat the measurement for channel B.

3.4.2.4. Normal/invert balance channel B (R647)

- Depress push-button B of the display mode switch S1.
- Depress the input coupling switch S15 (0).
- Check that the trace does not jump when PULL TO INVERT B switch S4 is switched between normal and invert. If necessary readjust R647 (Fig. 3.3.).

3.4.2.5. Shift balance (R547, R647)

- Depress push-button A (B) of the display mode switch S1.
- Depress push-button A (B) of the trigger source selector switch S16.
- Depress the input coupling switch S12 (S14) (AC).
- Release the input coupling switch S13 (S15) (0).
- Set the AMPL/DIV switch S6 (S8) to 20 mV/div and AMPL/DIV potentiometer R7 (R8) to CAL.
- Set the TIME/DIV switch S10 to 50 µs/div and TIME/DIV potentiometer R9 to CAL.
- Apply a sine-wave voltage of 480 mVp-p, 10 kHz, to the A (B) input socket.
- Check if te extremes of the sine-wave can be displayed distortion free on the screen by rotating the POSITION potentiometer R2 (R3). If necessary readjust potentiometer R547 (R647) (see Fig. 3.3.).
- Repeat the measurement for channel B.

3.4.3. Trigger balance (R356, R358, R361)

- Depress push-button A of the display mode switch S1.
- Set X MAGN switch S5 to position X1.
- Set TIME/DIV switch S10 to 0.1 ms/div and TIME/DIV potentiometer R9 to CAL.
- Depress push-button AUTO of the trigger mode switch S2.
- Set X POSITION potentiometer R4 so that the time base line starts at the most left graticule line.
- Set TIME/DIV switch S10 to DEFL.
- Depress push-button EXT of the trigger source selector switch S16.
- Check that the spot is in the center of the screen; tol. 1 div.
- Depress push-button A of the trigger source selector switch S16.
- Depress push-button DC of the trigger mode switch S2.
- Check that the spot is in the center of the screen.
  If necessary readjust potentiometer R356 (Fig. 3.2.).
- Depress push-button B of the trigger source selector switch S16
- Check that the spot is in the center of the screen.
  If necessary readjust potentiometer R361 (Fig. 3.2.).
- Depress both A and B push-bottons (composite) of the trigger source selector switch S16.
- Shift the spot to the central horizontal graticule line using A POSITION potentiometer R2.
- CHECK that the spot is in the center of the screen.
  If necessary readjust potentiometer R358 (Fig. 3.2.).

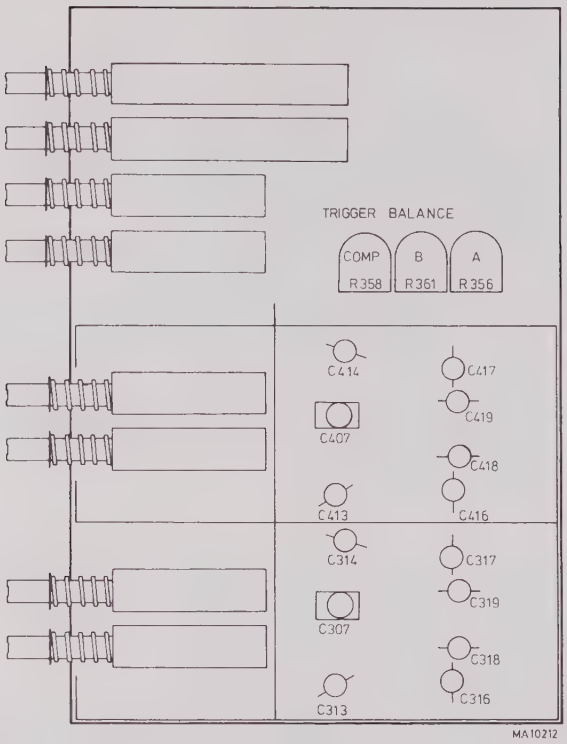


Fig. 3.2. Adjusting elements attenuator board

3.4.4. Time coefficients (R1417, R1419, R1232)

- Depress push-button A of the display mode switch S1.
- Depress push-button AUTO of the trigger mode switch S2.
- Set X MAGN switch S5 to position X1.
- Set A AMPL/DIV switch S6 to 20 mV/div.
- release the input coupling switch S13 (0)
- Depress push-button A of the trigger source selector switch S16.
- Set TIME/DIV switch S10 to 2 µs/div and TIME/DIV potentiometer R9 to CAL.
- Apply a time marker voltage with repetition time of 2 µs and an amplitude of 80 mVp-p to the A input socket X2.
- Check that the central 8 cycles occupy 8 divisions.
  If necessary readjust potentiometer R1417 (Fig. 3.3.).
- Pull X MAGN switch S5 to position X10.
- Change the repetition time of the applied input signal to 0.2 µs.
- Check that the central 8 cycles occupy 8 divisions.
  If necessary readjust potentiometer R1419 (Fig. 3.3.).
- Check that the trace can be shifted over 100 divisions with the aid of X-POSITION potentiometer R4.
- Push X MAGN switch S5 to position X1.

- Set TIME/DIV switch S10 to 5 ms/div.
- Change the repetition time of the applied input signal to 5 ms.
- Check that the central 8 cycles occupy 8 divisions.
  If necessary readjust potentiometer R 1232 (Fig 3.3.).
- Check all the other positions of the TIME/DIV switch S10. The repetition time of the applied input signal should correspond to the position of the TIME/DIVISION switch S10.
  The central 8 cycles should always occupy 8 divisions: tolerance + 1 subdivision (2 subdivisions with X MAGN switch S5 to position x10).
- Check that in all the positions of the TIME/DIV switch S10 the time-base length is at last 10 divisions.
- Check the control range of the TIME/DIV potentiometer R9 in the position 0.1 ms/div of the TIME/DIV switch S10. This should be 1:$\geqslant$ 2.5.

3.4.5. Vertical amplifiers

3.4.5.1. General information

The adjustments of the vertical amplifier channels A and B are identical. The knobs, sockets and adjusting elements of channel B are shown in brackets after those of channel A.

3.4.5.2. Deflection sensitivity (gain)

The adjustments of the vertical amplifier sensitivity must follow the specified sequence.

Channel B	X1	Gain	(R848)
Channel A	X1	Gain	(R543)
Channel B	X10	Gain	(R621)
Channel A	X10	Gain	(R521)

Deflection sensitivity X1 (R848, R543)

- Depress push-button B (A) of the display mode switch S1.
- Depress button AUTO of the trigger mode switch S2.
- Depress push-button B (A) of the trigger source selector switch S16.
- Set AMPL/DIV potentiometer R8 (R7) to CAL.
- Release input coupling switch S14 (S12) (DC).
- Release input coupling switch S15 (S13) (0).
- Set TIME/DIV switch S10 to 0,2 ms/div
- Set AMPL/DIV switch S8 (S6) to 20 mV/div.
- Apply a square-wave voltage of 120 mV, frequency approx. 2 kHz, to the B (A) input socket.
- Check that the signal occupies 6 divisions.
  If necessary readjust potentiometer R848 (R543) (Fig. 3.3.).
- Repeat the measurement for channel A.

Deflection sensitivity X10 (R621, R521)

- Depress push-button B (A) of the display mode switch S1.
- Depress push-button AUTO of the triggermode switch S2.
- Depress push-button B (A) of the trigger source selector switch S16.
- Set AMPL/DIV potentiometer R8 (R7) to CAL.
- Release input coupling switch S14 (S12) (DC).
- Release input coupling switch S15 (S13) (0).
- Set TIME/DIV switch S10 to 0,2 ms/div
- Set AMPL/DIV switch S8 (S6) to 20 mV/div.
- Apply a square-wave voltage of 120 mVp-p, frequency approx. 2 kHz, to the B (A) input socket.
- Check that the signal occupies 6 divisions.
  If necessary readjust potentiometer R621 (R521) (Fig. 3.3.).

Repeat the measurement for channel A.

3.4.5.2.

- Depress push-button A (B) of the display mode switch S1.
- Depress push-button AUTO of the triggermode switch S2.
- Depress push-button A (B) of the trigger source selector switch S16.
- Set TIME/DIV switch S10 to 0,2 ms and the TIME/DIV potentiometer R9 to CAL.
- Release input coupling switch S12 (S14) (DC).
- Release input coupling switch S13 (S15) (0).
- Set AMPL/DIV switch R7 (R8) to CAL.
- Apply a square-wave voltage with an amplitude as indicated in the following table, a repetition rate of approx. 2 kHz and a rise time $\leqslant$ 100 ns, to the A (B) input socket.
- Check that no overshoot is visible (max. pulse top errors 2%), and check that the trace height is 6 divisions $\pm$ 3% (1 subdivision).

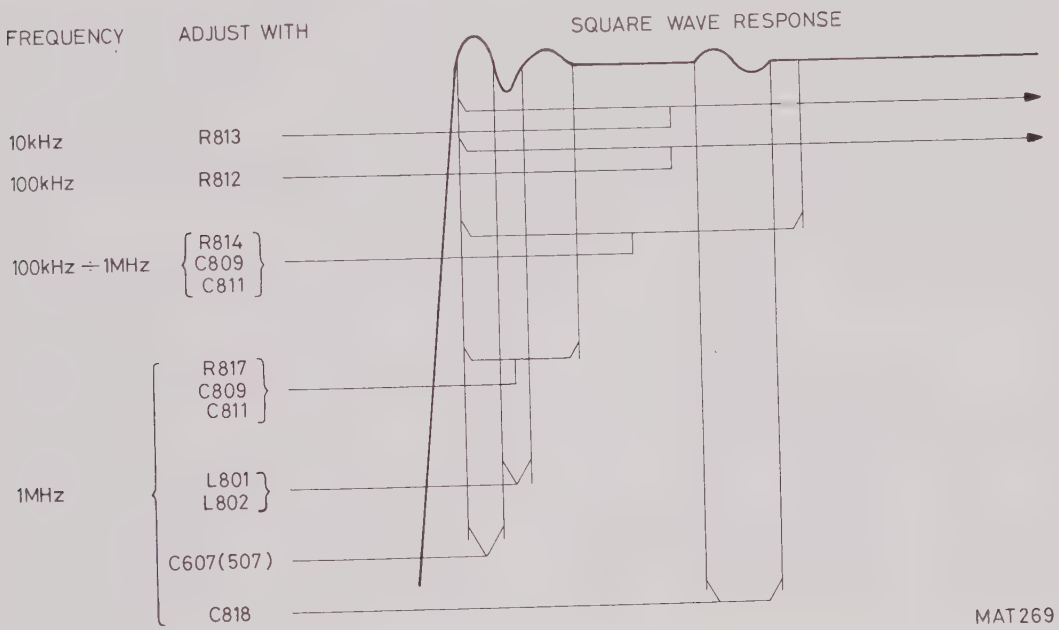
S6 (S8) ampl. to	Input signal	Adjust with
20 mV	120 mV	C307 (C407)
50 mV	0,3 V	C313 (C413)
0,1 V	0,6 V	C314 (C414)
0,2 V	1,2 V	C316 + C318 (C416 + C418)
2 V	12 V	C317 + C319 (C417 + C419)

- Repeat the measurement for channel B.

3.4.5.4. Square-wave response final amplifier

- Depress push-button A (B) of the display mode switch S1.
- Depress push-button AUTO of the trigger mode switch S2.
- Depress push-button A (B) of the trigger source selector switch S16.

- Push NORMAL/INVERT switch S4 to position NORMAL.
- Set B AMPL/DIV switch S8 to 20 mV/div and B AMPL/DIV potentiometer R8 to CAL.
- Apply a square-wave voltage of approx. 120 mVp-p, with rise time $\leqslant$ 3 ns, to the B input socket.The pulse repetition should be in accordance with the table below.
- Check the square-wave response, pulse top errors may not exceed 1 subdivision
- Check that the rise time does not exceed 14 ns.



* L801 and L802 should be operated simultaneously and in the same direction and by the same amount. If necessary repeat above adjustments until the best response is obtained.

- Check and readjust the square-wave response according to the table below.

Channel	Ampl/div	Input Signal	Trace height	Rep.rate	Time/div	Adj. with	Max.error
B	2 mV/div	12 mV	6 div.	1 MHz	0,2 µs	C602	1 subdivision
A	20 mV/div	120 mV	6 div.	1 MHz	0,2 µs	C508	1 subdivision
A	2 mV/div	12 mV	6 div.	1 MHz	0,2 µs	C502	1 subdivision

3.4.5.5. Cross talk (R813)

- Depress push-button CHOP of the display mode switch S1.
- Depress push-button AUTO of the trigger mode switch S2.

- Depress push-button B of the trigger source selector switch S16.
- Push NORMAL/INVERT switch S4 to position NORMAL.
- Set A and B AMPL/DIV switch S6 and S8 to 20 mV/div and the AMPL/DIV potentiometer R7 and R8 to CAL.
- Set the TIME/DIV switch S10 to 0,5 ms/div and the TIME/DIV potentiometer R9 to CAL.
- Depress the input coupling switch S13. (0)
- Apply a square-wave voltage of 120 mVp-p, with rise time $\leqslant$ 3 ns, and a repetition rate of approx. 10 kHz to the B input socket.
- Adjust potentiometer R813 (Fig. 3.3.) for minimum cross talk between channels.

3.4.5.6. Bandwidth check of channel A (B)

- Depress push-button A (B) of the display mode switch S1.
- Depress push-button AUTO of the triggermode switch S2.
- Depress push-button A (B) of the trigger source selector switch S16.
- Set TIME/DIV switch S10 to 0,1 ms/div and the TIME/DIV potentiometer R9 to CAL.
- Set AMPL/DIV switch S6 (S8) to 2 mV/div and AMPL/DIV potentiometer R7 (R8) to CAL.
- Release input coupling switch S12 (S14) (DC).
- Release input coupling switch S13 (S15) (0).
- Apply a sine-wave signal of 12 mVp-p, frequency approx. 100 kHz to the A (B) input socket.
- Increase the frequency of the input signal to 35 MHz, the amplitude of the signal must remain 12 mV.
- Check that the trace height is at least 4,2 divisions at input frequency of 35 MHz.

Repeat the measurement for channel B.

3.4.6. Triggering

3.4.6.1. Trigger slope (R1014)

- Depress push-button A of the display mode switch S1.
- Depress push-button AUTO of the triggermode switch S2.
- Depress push-button A of the trigger source selector switch S16.
- Depress input coupling switch S13 (0).
- Set LEVEL potentiometer R5 to its midposition.
- Check with a multimeter that the DC output voltage of the trigger amplifier (collector of V1014) does not change if SLOPE push-button S3 is switched between + and -. If necessary readjust potentiometer R1014 (Fig. 3.3.).
- Set AMPL/DIV switch S6 to 20 mV/div and AMPL/DIV potentiometer R7 to CAL.
- Release input coupling switch S12 to (DC).
- Release input coupling switch S13 (0).
- Apply a sine-wave signal of 120 mVp-p, frequency approx. 2 kHz to the A input socket.

- Set TIME/DIV switch S10 to 0,2 ms/div.
- Release SLOPE switch S3 to the + position and check that the trace starts with a positive going edge.
- Depress SLOPE switch S3 to the - position and check that the trace starts with a negative going edge.

3.4.6.2. Trigger sensitivity (R1041)

- Set the controls as on the previous section.
- Apply a sine-wave signal of 120 mVp-p, frequency approx. 2 kHz to the A input socket.
- Find the lowest possible input signal at which it is still possible to obtain a triggered trace with the aid of LEVEL potentiometer R5 and potentiometer R1041 (Fig. 3.3.).

3.4.6.3. Trigger level internal DC

- Depress push-button A of the display mode switch S1.
- Depress push-button DC of the trigger mode selector switch S2.
- Depress push-button A of the trigger source selector switch S16.
- Apply a sine-wave signal for a trace height equivalent of 16 divisions to the A input socket.
- Check that the starting point of the sine-wave can be shifted across 16 divisions with the aid of LEVEL potentiometer R5.
- Enlarge the vertical deflection to 24 divisions and check that the level range of R5 does not exceed 24 divisions.

3.4.6.4. Trigger level auto

- Depress push-button A of the display mode switch S1.
- Depress push-button DC of the trigger mode selector switch S2.
- Depress push-button A of the trigger source selector switch S16.
- Release input coupling switch S13 (0).
- Apply a sine-wave voltage at a frequency of approx. 100 Hz for 6 divisions trace height to the A input socket.
- Check that the starting point of the sine-wave can be shifted across approx. 3 divisions with the aid of LEVEL potentiometer R5.

3.4.6.5. Trigger level external

- Depress push-button A of the display mode switch S1.
- Depress push-button AC of the trigger mode selector switch S2.
- Depress push-button EXT of the trigger source selector switch S16.
- Release input coupling switch S12 (DC).
- Release input coupling switch S13 (0).
- Set A AMPL/DIV switch S6 to 1 V/div and A AMPL/DIV potentiometer R7 to CAL.

- Set TIME/DIV switch S10 to 0,2 ms/div. and TIME/DIV potentiometer R9 to CAL.
- Apply a sine-wave signal of 8 Vp-p,frequency of approx. 2 kHz to the A and EXT input sockets.
- Check that the starting point of the sine-wave can be shifted across the entire amplitude of the signal with the aid of LEVEL potentiometer R5.

3.4.6.6. Trigger sensitivities

- Check that the trigger sensitivity is in accordance with or is better then the specifications in the table below.

Trigger source S16	Trigger mode S2	+/- S3	Trace height or ampl.	Signal to	Freq.	Shape	Ampl. input voltage
A	Auto	+	1 div.	X2 (YA)	100 Hz	Sine	20 mVp-p
A	Auto		1 div.	X2 (YA)	10 kHz	Sine	20 mVp-p
A	Auto		1 div.	X2 (YA)	35 MHz	Sine	28 mVp-p
A	AC		1 div.	X2 (YA)	20 Hz	Sine	20 mVp-p
A	AC		1 div.	X2 (YA)	35 MHz	Sine	28 mVp-p
A	DC		1 div.	X2 (YA)	35 MHz	Sine	28 mVp-p
B	DC		1 div.	X3 (YB)	20 Hz	Sine	20 mVp-p
B	DC		1 div.	X3 (YB)	35 MHz	Sine	28 mVp-p
A+B	DC		1 div.	X3 (YB)	35 MHz	Sine	28 mVp-p
A+B (compl) (S1 in ALT)	DC			X2 (YA) X3 (YB)	$\pm$ 2 kHz $\pm$ 2 kHz	Square* Sine*	$\pm$20 mVp-p $\pm$20 mVp-p
B	TV	+	0,7 div. Sync. pulse	X3 (YB)		+ Video	14 mVp-p Sync. pulse
B	TV	-	0,7 div. Sync. pulse	X3 (YB)		- Video	14 mVp-p Sync. pulse
B	TV	-	$\pm$ 2 div. Sync. pulse	X3 (YB)		- Video	$\pm$40 mVp-p Sync. pulse
EXT	DC		0,2 Volt.	X4 (EXT)	20 Hz 35 MHz	Sine Sine	0,2 Vp-p 0,2 Vp-p
EXT 10	DC		2 Volt.	X4 (EXT)	20 Hz 35 MHz	Sine Sine	2 Vp-p 2 Vp-p

* originating from different sources

- Set LEVEL potentiometer R5 as required.
- Set TIME/DIV switch S10 so that a reasonable number of sine-waves is displayed.
- Set A and B AMPL/DIV switches S6 and S8 to 20 mV/div. an the A and B AMPL/DIV potentiometers R7 and R8 to CAL.

3.4.7.X-Deflection

3.4.7.1. Sensitivity

- Set TIME/DIV switch S10 to X DEFL.
- Depress push-button EXT of the trigger source selector switch S16.
- Apply a sine wave voltage of 4 Vp-p frequency approx. 10 kHz, to socket EXT.
- Check that the trace length is 8 divisions ± 0,8 division.

3.4.7.2. Frequency response

- Set TIME/DIV switch S10 to X DEFL.
- Depress push-button EXT of the trigger source selector switch S16.
- Apply a sine wave voltage of 4 Vp-p (trace length 8 divisions) frequency approx. 10 kHz, to the EXT input socket.
- Increase the frequency to 1 MHz.
- Check that the trace length is at least 5,6 divisions.

3.4.7.3. Horizontal sensitivity via input A

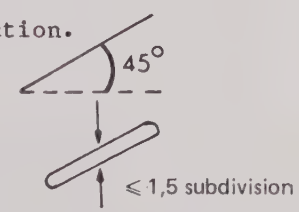
- Set A AMPL/DIV switch S6 to 20 mV/div and A APML/DIV potentiometer R7 to CAL.
- Depress push-button B of display mode switch S1
- Set TIME/DIV switch S10 to X DEFL.
- Depress push-button A of the trigger source selector switch S16.
- Apply a sine wave voltage of 120 mVp-p frequency approx. 2 kHz, to the A input socket.
- Check that the trace length is 6 divisions ± 0,6 division.

3.4.7.4. Horizontal sensitivity via input B

- Set B AMPL/DIV switch S8 to 20 mV/div and B APML/DIV potentiometer R8 to CAL.
- Depress push-button A of display mode switch S1
- Set TIME/DIV switch S10 to X DEFL.
- Depress push-button B of the trigger source selector switch S16.
- Apply a sine wave voltage of 120 mVp-p, frequency approx. 2 kHz, to the B input socket.
- Check that the trace length is 6 divisions ± 0,6 division.

3.4.7.5. Phase difference between X and Y channels

- Input signal and control settings as in the previous section.
- Depress push-button B of the display mode switch S1.
- Check that the line is displayed under an angle of 45°
- Increase the frequency to 100 kHz.
- Check that the phase error does not exceed 3° division.



3.4.8.Calibration voltage (R1607)

- Check that the voltage on the CAL output socket is 1,2 V ± 1%. If necessary readjust potentiometer R1607 (Fig. 3.3.).

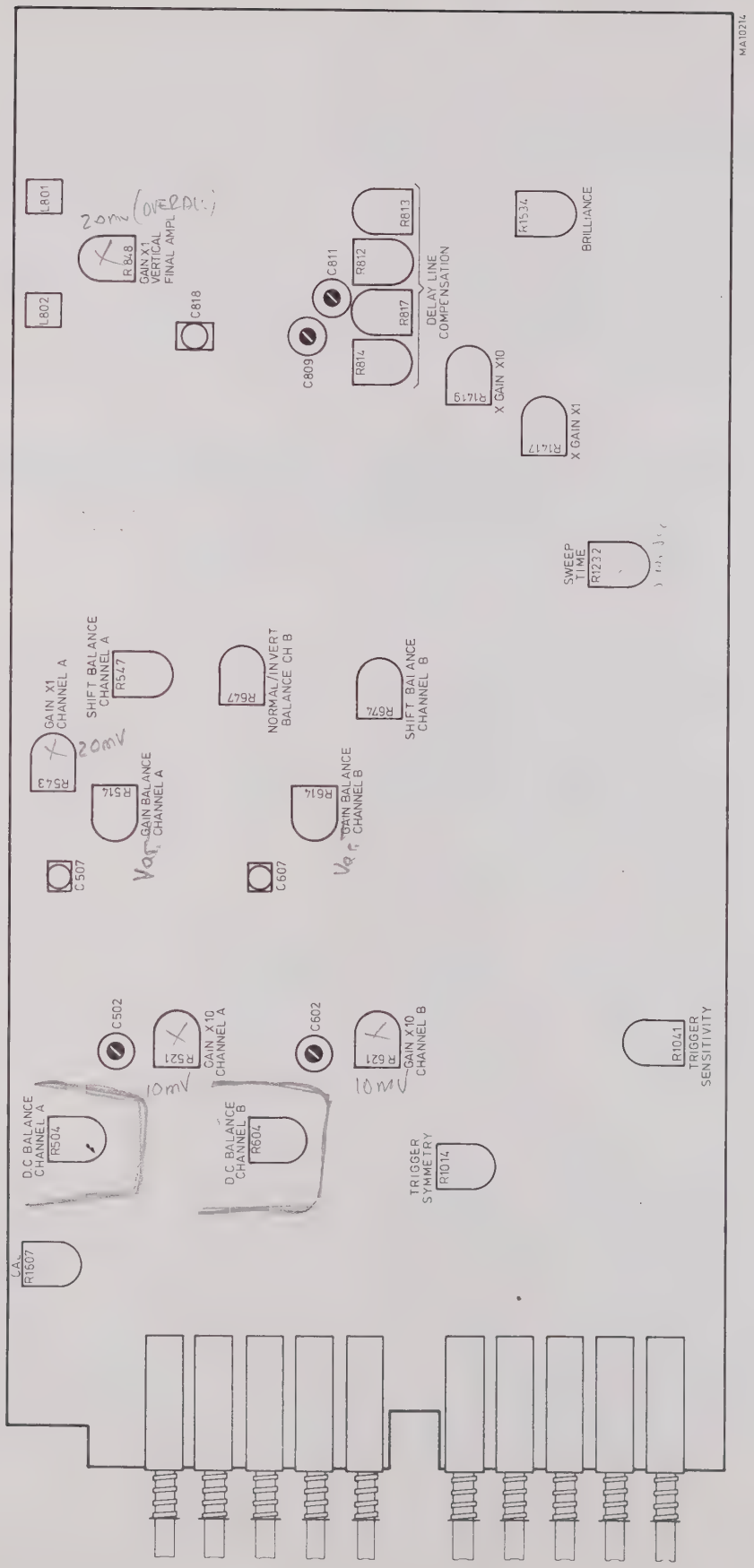


Fig. 3.3. Adjusting elements amplifier board

3.5. Analyzer section

- Pushbutton LSA/OSC (S19) depressed.

3.5.1. Intensity

- Depress pushbutton DATA (S33)
- Depress pushbutton "1" (S34)
- Adjust the intensity by potmeter R15.

3.5.2. Vertical size of display

- Depress pushbutton DATA (S33)
- Depress pushbutton "1" (S34)
- Adjust potmeter R2140 until the vertical size of the displayed data is 7,6 ± 0,4 div.

3.5.3. Horizontal and vertical position

- Depress pushbutton DATA (S33)
- Depress pushbutton "1" (S34)
- Shift vertical position by potmeter R13
- Shift horizontal position by potmeter R14

3.5.4. Threshold voltages

- Selectable between -3 ... +12 V
- THRESHOLD tumbler switch in position VAR1
- measure threshold between MEAS pin´s (X14 - X15)
- adjust threshold by potmeter R16
- THRESHOLD tumbler switch in position VAR2
- measure threshold between MEAS pin´s (X14 - X15)
- adjust threshold by potmeter R17.
- THRESHOLD tumbler switch in position TTL
- check TTL level +1,4 V between MEAS pin´s (X14 - X15)

3.5.5. System-clock SYCKP

- Connect a pod PM 8821 to each data input socket X10, X11 and X12
- interconnect the data inputs of the three pods.
- select the following parameters : CK0 Q0 Q1 Q2 = 1xxx CK1 Q0 Q1 Q2 = xxxx
  TRIG = 1 1111 1111 0000 0000 0000 DCK0
  DATA = S DLY = 00126S
- apply a square wave signal, repetition time 4 µsec and pulse width 500 nsec, to clock 0 input (pod 2 channel 7)
- press START/STOP (S21)

- check SYCKP on test point T16
- apply a square wave signal, repetition time 100 nsec and pulse width 25 nsec, to clock 0 input (pod 2 channel 7)
- check on test point T16 if SYCKP is still present
- apply a square wave signal, repetition time 8 usec and pulse width 1 µsec, to clock 0 input (pod 2 channel 7)
- adjust the SYCKP pulse width on 55nS + 3 nS with capacitor C 2479.

3.5.6. Hold time of the data input channels (adjusting capacitors: C2307, 2308, 2327, 2391, 2332, 2328, 2331, 2333, 2378, 2381, 2383, 2379, 2382, 2384, 2419, 2421, 2422, 2423, 2424, 2426, 2427 and 2428 to the left to get a minimum delay of the captured data)

- select the following parameters :
  CK0 Q0 Q1 Q2 = 1xxx CK1 Q0 Q1 Q2 = xxxx
  TRIG = x xxxx xxxx xxxx xxxx xxxx D CK0
  DATA = S DLY = 00126S
- apply square wave signal, repetition time 5 µs and pulse width 5 µs, to both the interconnected data inputs and the clock 0 input (pod 2 channel 7)
- depress AUTO/MAN (S20)
- press START/STOP (S21)
- display picture : (only "1" ´s)
- adjust the above listed capacitors untill the next displays appears (only "0"´s). The hold time now is $\leqslant$ 0 nsec.

3.5.7. Set-up time of data input channels

- select the following parameters:
  CK0 Q0 Q1 Q2 = 0xxx CK1 Q0 Q1 Q2 = xxxx
  TRIG = x xxxx xxxx xxxx xxxx xxxx DCK0
  DATA = S DLY = 00126S
- apply a square-wave signal, repetition time 500 nsec and pulse width 500 nsec to the interconnected data inputs and the clock 0 input (pod 2 channel 7)
- depress AUTO/MAN (S20)
- press START/STOP (S21)
- display picture : only "1" ´s
- adjust the capacitor´s listed in 3.5.6. until just ones are captured. Set up time now is $\leqslant$ 35 nsec. See display picture.
- check again the hold time 3.5.6.

3.5.8. Hold time of trigger qualifier

- select the following parameters :
  CK0 Q0 Q1 Q2 = 1xxx CK1 Q0 Q1 Q2 = xxxx
  TRIG = xx xx xx QD CK0
  DATA = S TRIGQ = 0 DLY = 00126S
- apply a square-wave signal, repetition time 1 µsec and pulse width 500 nsec, to clock 0 input (pod 2 channel 7) and via probe PM 8925 to the BNC input-socket TRIGQUAL (X5).
- adjust capacitor C 2307 until the analyzer is triggered.

3.5.9. Set-up time of trigger qualifier

- select the following parameters
  CK0 Q0 Q1 Q2 = 1xxx CK1 Q0 Q1 Q2 = xxxx
  TRIG = xx xx xx QD CK0
  DATA = S TRIG Q = 0 DLY = 00126S
- apply a square-wave signal, repetition time 1 µsec and pulse width 500 nsec, to clock 0 input (pod 2 channel 7) and via probe PM 8925 to the BNC input socket TRIGQUAL (X5)
- adjust capacitor C2307 until the analyzer is just triggered.
  set up time is now $\leqslant$ 25 nsec.
- check again the hold-time 3.5.8.

4. INFORMATION TO ASSIST IN FAULT FINDING

4.1. General information

The following information is provided to facilitate troubleshooting.
Information contained in other sections of this manual should be used allong with the following information to aid in locating the defective component. An understanding of the circuit operation is necessary for locating troubles.

4.2. Power supply

The available unloaded voltage tappings and the number of turns per winding are listed in the circuit diagram, fig. 7.13. in the form of a table.

4.3. Troubleshooting in the oscilloscope section

The d.v. voltage levels at the electrodes of the transistors and the voltage wave-forms in the time-base generator are shown at the relevant points on the circuit diagram (fig. 7.13.)
The logic scope under test must be set in the following way to measure the voltage wave-forms as shown in fig. 7.13.
- select the OSC mode
- X-POSITION potentiometer RU at mid-range
- A-POSITION potentiometer R2 at mid-range
- LEVEL potentiometer R5 at mid-range
- SLOPE switch in position "+"
- TRIGGER source selector switch S16 in position A
- A and AUTO push-buttons S1A and S2A depressed.
- A AMPL/DIV switch S6 to 1V/div and potentiometer R7 to CAL
- TIME/DIV switch S10 to 0,2/div., potmtr. R9 to CAL and X MAGN switch S5 to X1
- Input signal on A input socket X2 : 2,5 kHz sine-wave voltage of 8 div. deflection

4.4. Trouble shooting in the analyzer section

4.4.1. General information

The Logic Scope is provided with a service test program by which the analyzer section can be tested and occuring failures can be traced.
The Service test program can only be used if the following parts operate.
- Power supply. For checking the power supply (for oscilloscope and analyzer) see figure 7.13.
- Deflection circuits of CRT. These circuits can be tested in the oscilloscope mode. See chapter 4.3.
- Microprocessor and microprocessor busses : address bus, data bus and control bus. If the bus lines are checked with an oscilloscope in general a very unstable display will be the result. This is due to the fact that these

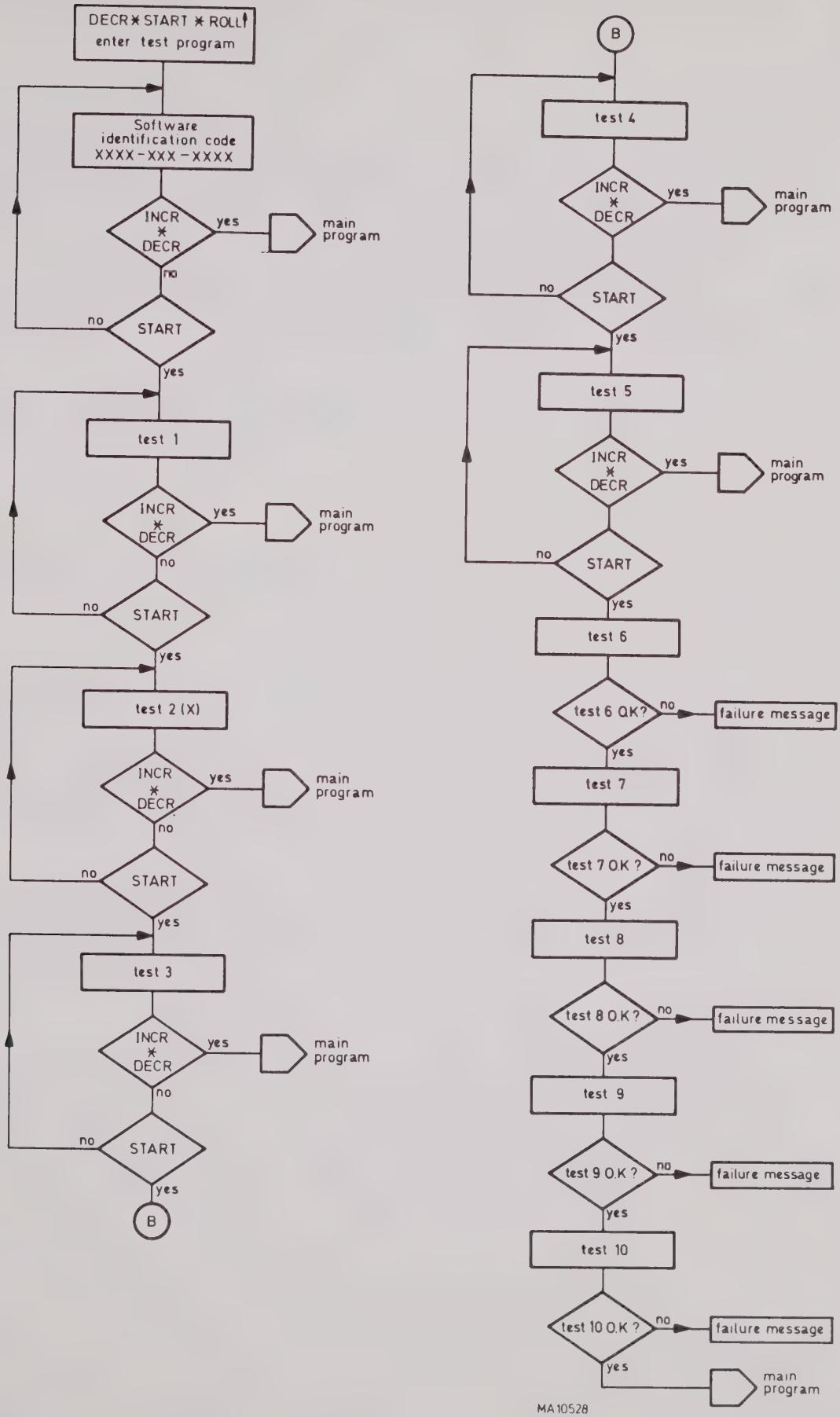


Fig. 4.1. Flow chart of the sequence of service selftests

signals vary with time in rather unpredictable way. If anyhow stable display of signals from one of these busses is obtained,this may be an indication that the microprocessor runs in a small program loop. Check the busses. If one of the bus lines show no activity this might indicate a shortage to ground or + 5V. If there is no activity on the busses at all the microprocessor doesn´t run. Exchange the microprocessor.

- EPROM´s. The EPROM´s contain the program on which the microprocessor operates. Also the testprogram is stored in these EPROM´s. Failing EPROM´s can be the cause of all kind´s of failures. In case their is a doubt the functioning of the EPROM´s exchange them by a known well functioning pair.

NOTE : In the testprogram of the PM 3542 the Decoder tests (test 2, 3 and 4) are left out. Be aware that therefore the numbers of the test have been changed compared to this description.

4.4.2.Service test program

The Logic Scopes PM 3543 and PM 3542 are provided with a service test program by which the abalyzer section can be tested and occuring failures can be traced. The service test can be selected by pressing DECR/0, holding ROLL up and pressing START. Then the Software Identification, see chapter 1.2., is displayed on the screen.By pressing START/STOP again the first test is selected. The flow chart in Fig. 4.1. indicates how the several tests can be selected. In test 1, 2, 3, 4 and 5 the microprocessor applies a square-wave signal to the input of the component to be tested. The functioning of the component can be checked with an oscilloscope .The oscilloscope of the logic scope itsself can be used to check these components, but therefore the hold state of the microprocessor must be removed, by connecting pin 1 of pushbutton S36 (DECR/0) to ground. During normal operation the microprocessor is kept in the hold state when the oscilloscope is selected in order to eliminate the possibility of interference between analyzer and oscilloscope.
By tests 6, 7, 8, 9 and 10 a great part of the circuit is automatically tested and when no failures occur the tests are, automatically, executed in sequence and the microprocessor jumps to the main program. If failures occur in a test the program stops in that particular test and an indication of the failure is displayed on the screen. For operating the service test program :

- no external connections must be .
- jumper Q2391 must be replaced from W1 (normal) to W2 (test)
- if the built in oscilloscope is used to check the analyzer S36 pin 1 must be connected to ground.

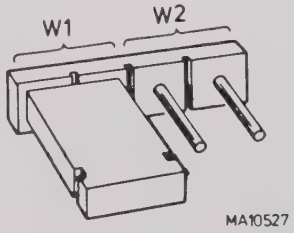


Fig.4.2. Front view of the jumper connection

4.4.3. Survey of the tests

Test 1 until 4 are not available in the PM 3542.

Test 1 : Interface oscilloscope
Test 2 : Decoder D2323
Test 3 : Decoder D2311
Test 4 : Decoder D2321
Test 5 : Programmable Peripheral Interface D2303
Test 6 : Address Counter (D2354 and D2357), Address Pointer (D2327) and clock CKO
Test 7 : Clock CK1
Test 8 : Data Acquisition Memories (D2319, D2328, D2341, D2342, D2358, D2369) and Programmable Peripheral Interface D2318
Test 9 : System test
Test 10: External trigger-qualifier test

4.4.4. Description of the tests

Test 1

The ASCII Latches D2111 and D2112 and the Vertical Latch D2118 are alternately, with a frequency of 30 Hz, loaded by microprocessor with 0101 0101 and 1010 1010.
When the ASCII Latches are loaded with 1010 1010 character * (ASCII code 1010 1010) is displayed at the left side at the top of the screen.
This position is determined by the value stored in the Vertical Latch(101010) and the initial value 0010 1010 (=42D) of the horizontal positioning counters D2102 and D2101.
When the ASCII Latches are loaded with 0101 0101 nothing is displayed on the screen because the Fast Blank signal is 1 which inhibits the 47-counter to generate a character.
By means of an oscilloscope the interface oscilloscope circuitry can be tested while this test is running.

Test 2

DECODER D2323 is used to decode control and selection signals,
out of address lines A12, A13, A14 and A15. Behind the number of the test is a number displayed which indicates which output of the decoder is tested.
At the selected output can, by means of an oscilloscope, a square-wave signal be measured which is generated by the microprocessor.
By pressing START the next output can be tested.
NOTE: on outputs 0, 1, 7 and 14 are always signals present.

Test 3

DECODER D2311 is used to decode control signals out of adress lines A0, A1 and A2. This DECODER can be checked on the same manner as DECODER D2323 however only outputs 7, 6, 5, 4 and 1 need to be checked.
NOTE: On outputs 7 and 1 are always signals present.

Test 4

DECODER D2321 is used to decode control signals out of the address lines A0 and A1. This DECODER can be checked on the same manner as D2323.
NOTE: On output 2 is always a signal present.

Test 5

The Programmable Peripheral Interface D2303 is alternately loaded with a frequency of 30 Hz with 1010 1010 and 0101 0101 .
These signals can be checked on the output ports PA, PB and PC of the PPI by means of an oscilloscope.

Test 6

The Address Counter (D2354 MSC and D2357 LSC) is loaded by microprocessor with 0101 0101. This load operation is checked by microprocessor via the Address Pointer. Next, the Address Counter is loaded with 1010 1010 and this is also checked by the uP.
After the Address Counter is loaded the microprocessor generates, by alternately changing the polarity of CK0, 256 clock pulses. Out of these clock pulses the CKAC is generated.
The microprocessor checks continuously, via the Address Pointer, the values at the outputs of the Address Counter.
If the Address Counter fails the failing address is displayed on the screen.
The test uses the CK0 selection and the CKAC circuit so these sections are also tested.

Test 7

The microprocessor generates, by changing the polarity, one clock pulse CK1 and checks if the Address Counter is incremented. If the Addres Counter is not incremented on the screen is displayed "TEST 7 FAILS" which indicates a failure in the clock circuit.
If failures occur the test is continuously repeated, and the clock circuit can be tested with an oscliioscope.

Test 8

The Data Acquisition Memories are, via PPI1, by the microprocessor loaded with 555555H. The DAM´s are addressed by the microprocessor via the Address Counter. After the DAM´s are loaded the microprocessor checks the contents by reading them.
A simular operation is executed with AAAAAAH.
If the failure occurs on the screen is e.g. displayed:
"TEST 8 0000 0001-0".
The value of the last digit indicates:
"0" : failure in DAM0...DAM7
"1" : failure in DAM8...DAM15
"2" : failure in DAM16...DAM23
The "1" in the displayed byte, indicates the failing node.
A failing node can be caused by :
- DAM bus shortage
- failing Data Acquisition memories
- failing PPI 1

Test 9

The Delay Counters (D2367, D2374, D2363 and D2366) are loaded, by the microprocessor with 1000H.
The Trigger Memories (D2309, D2326, D2339) are loaded with don´t cares.
The microprocessor generates the SYCKP. The parallel triggermode is selected.
The microprocessor generates 1002H pulses; on the screen is displayed the value the Delay Counter should have.
When the system has not triggered after 1002H pulses on the screen is displayed 0000H.
The actual value of the Delay Counter (measured e.g. with an oscilloscope) gives an indication of the failure.

Test 10

In order to test the External Trigger-qualifier circuitry the selection signals SQTW1 and SQTW2 are set to 1.
The polarity of the qualifier PQTW is made 1 and the microprocessor checks if TWCK0 remains 0.
In case of a failure behind the test number is displayed a 0.
Next the polarity is set to 1 and the microprocessor checks if TWCK0 becomes a 1. In case of a failure behind the test number is displayed a 1.

4.4.5.Trouble shooting hints

4.4.5.1. Interface oscilloscope

- No display	- check power supply - check CRT and deflection circuit - check horizontal and vertical positioning - check character blanking signal - check output 8 of OR-gate D 2114 - check oscillator (2,4 MHz) - check signal CHARDY
- deformed characters	- check 47- counter - check column scanner - check horizontal and vertical positioning
- wrong characters	- check ASCII Latches - check character Generator

4.4.5.2. Address Counter and clock ciruit

Using test 6 to the following indicators can occur.

TEST 6 01010101
- check if jumper Q 2301 is in the test position. See fig. 4.2.
- check if the Address Counters are loaded check signal SDAMAC
- check the clock circuit. This can be done in the normal operating mode by applying a signal to the CKO input and selecting a triggerword that will not appear.
  Like this SYCKP is continuously generated.
  Then the clock circuit can be checked by means of an oscilloscope.

TEST 6 01011111
- check nand gate D2332

4.4.5.3. Data Input Latches, Data Acquisition Memories

The input circuit can also be checked without using the test program.
- connect the pod´s to the input data OAAAAA H
- select triggerword that doesn´t appear e.g. OFFFFF H
- apply a clock signal to the clock 0 of input (pod 2 channel 7)
- start the data acquisition
- check the Data Input Latches with an oscillscope.
- stop the data acquisition
- check the contents of the DAM´s which is displayed on the screen.
- follow the same procedure by connecting the pod´s to input data 155555 H

4.4.5.4. Trigger Control Circuit and Delay Counters

The Trigger Control Circuit and Delay Counters can be checked during the normal operation, without using the testprogram.

- Apply input data to the data inputs
- select the triggermode to be checked
- select triggerword(s) that doesn´t appear during data acquisition
- select a delay
- apply a clocksignal to the clock 0 and/or clock 1 input
- start the data acquisition
- check the control signals on the output of PPI 2 with an oscilloscope.
- check the contents of the Delay Counter with an oscilloscope.
- check CKAC and CKDLYC
- check the status of the different signals in the Trigger Control ciruit

Note: This procedure can be followed in each triggermode.

4.4.5.5. Information about trouble shooting equipment

- Though most of the test measurements can be carried out with a 2-channel oscilloscope, use of a 4-channel oscilloscope (e.g. PM 3244 or PM 3264) or an analyzer (e.g. PM 3543 is recommended).
- Logic pulser, used to check simple in-circuit functions of integrated circuits.
- Logic indicator probe.
- Current tracer probe, to detect and to trace short circuit current on p.c. boards.

Use of digital logic trouble shooting instruments

Connect a pulser probe to an input of a logic circuit.Check the function of the circuit by connecting the indicator probe alternately to the input and the output of a circuit (see Fig. 4.3.). Always compare output with respect to input.

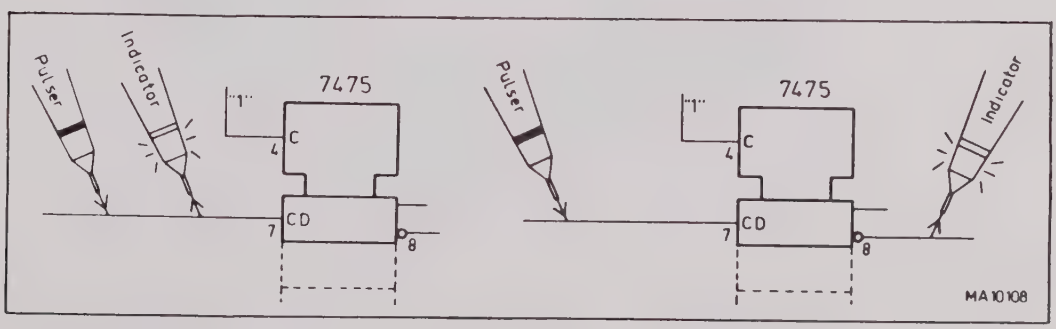


Fig. 4.3. use of logic pulser and indicator probes

Remarks

In case of a defect it is always possible to apply to the world wide PHILIPS Service Organization.
When the instrument is to be sent to a PHILIPS Service Workshop for repair, the following points should be observed:
- Attach a label with your name and address to the instrument.
- Give a complete description of the faults found, or the service required.
- Use the original packing, or, if this is no longer available, carefully pack the instrument in a wooden crate or box.
- Send the instrument to the address obtained after consultation with the local PHILIPS Organization.

5.DISMANTLING THE INSTRUMENT

5.1.General information

WARNING: This instrument must be disconnected from any voltage source before covers are removed.

This section describes the procedures necessary for the replacement of components during repair operations. All circuit boards removed from the unit should be adequately protected against damage and workshop practice of a high quality should be observed, during dismantling procedures a careful note must be made of any disconnected cables and plugs so that they may be correctly reconnected when the unit is reassembled. Damage may result if the unit is switched on after a circuit board has been removed or if a circuit board is removed within one minute of switching off.

5.2.Removal of instrument covers

The unit is protected by three covers: a front panel protecting cover, a wrap around cover with carrying handle and a rear panel on which the mains input transformer is mounted. To remove wrap around cover and rear panel first ensure that the front cover is in position.

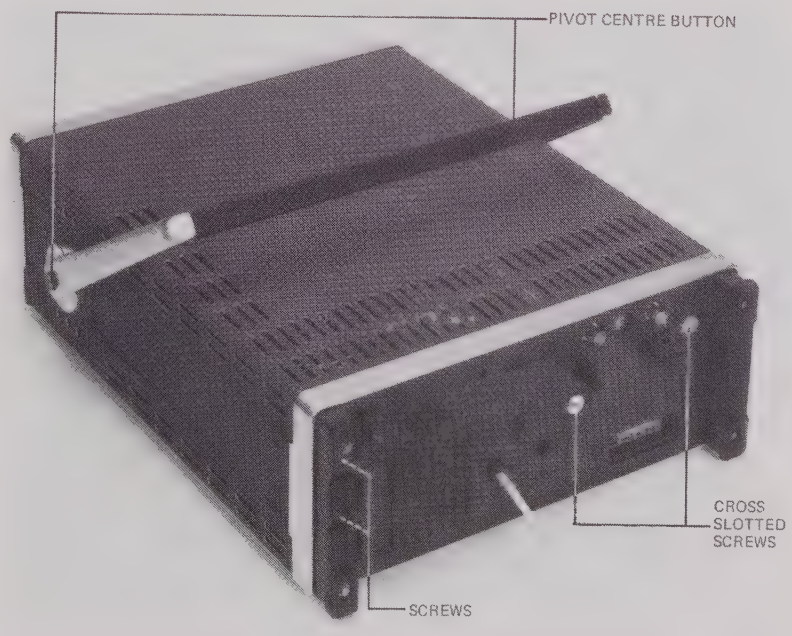


Fig.5.1. Removing the instrument covers

Then proceed as follows:
- Push both pivot centre buttons of the carrying handle and hange it clear of the front cover.

- Stand the unit on the front cover on a flat surface.
- Slacken the two coin slot screws located on the rear panel (Fig. 5.1.).
- Lift the rear panel and unplug the connector on power supply printed circuit board.
- Lift off the wrap round cover.
- For access to the front panel, stand the unit horizontally and snap off the front cover.

5.3. Removal of carrying handle

- Prise off centre knob from each pivot using a screwdriver (Fig. 5.1.). in one of the small slots in the side of the knobs.
- Remove the cross-slotted screws that are now accessible.
- Spring both arms slightly outwards and remove.
- Grip and arms are ordered separately (see list of mechanical parts), and a complete handle can be readily constructed by pushing the arms into the grip.

5.4. Removal of Bezel and contrast filter

- Take hold of the bezel´s bottom corners and gently pull it from the front panel (Fig. 5.2.).
- The contrast filter can be removed by pressing it gently out of the Bezel.

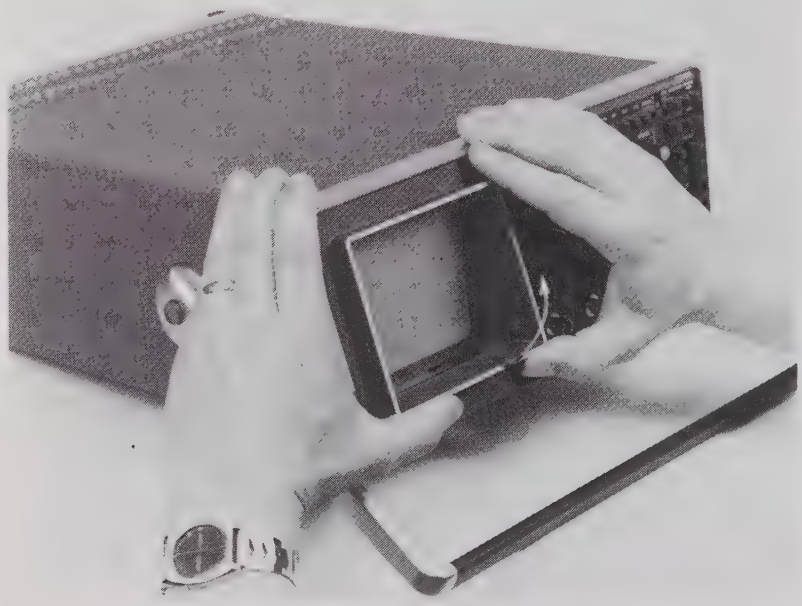


Fig.5.2. Removing the bezel and the contrast plate

5.5. Removal of control knobs and text plate

- The AMP/DIV and TIME/DIV knobs can be removed after pulling off the small knobs and then unscrewing the hexagon nuts.

- The "X" position and "B" position knobs are removed by prising of the knob cap and undoing the slotted nut that is then accessible.
- The remaining small knobs can then be pulled off of the shafts.
- The earth terminal nut must then be removed.
- The test plate can be removed after the three hexagon nuts from the AMP/DIV and TIME/DIV switches have been unfastened.

5.6.Removal and replacement of the C.R.T. and the tube screen

- Remove unit covers and rear panel (section 5.2.).
- Remove bezel and contrast filter (section 5.4.).
- Unplug connections on C.R.T. neck.
- Ease base socket off C.R.T.
- Slacken C.R.T. neckbrace.
- Unplug the trace rotation coil connector on the main amplifier board and pull cable and plug through the elongated hole in the centre frame.
- Withdraw the C.R.T. through the front panel until the E.H.T. connector is accessible.
- Remove the E.H.T. connector.
- Pass the C.R.T. right throught the front panel taking care with the cable and plug of the trace rotation coil.
- The tube screen can now be removed by unfastening the two retaining screws on the rear panel.
- Installation is in reverse order, position the C.R.T. screen flush with the contrast filter.
- The torque applied to the screw of the brace around the C.R.T. neck must be between 0.4 and 0.6 Nm.

5.7.Removing the front assembly

In order to gain access to parts on the AMPL/DIV switches, to replace trimmer capacitors or other components on the attenuator board, it is best to remove the front panel assembly as a whole in accordance with the following procedure.

- Remove the instrument covers in accordance with section.
- Remove the INTENS, FOCUS and ILLUM knobs by pulling them off the shaft.
- Remove the earthing terminal at the front.
- Remove the three screws A and B (Fig. 5.3.).
- Remove the three screws E that hold the attenuator board to the frame bar (Fig. 5.4.).
- Remove the three screws C (Fig. 5.3.).
- Make a note of the positions of the miniature socket connections on the amplifier board.
- Remove all plugs, miniature sockets, coaxial sockets and clamping terminals from unit and amplifier board.
- Remove the complete front assembly from the instrument: screening covers can then be removed to gain access to and remove parts.
- When the front panel assembly is reinstalled, make sure not to interchange the connections of the Y position controls. The connections are correct when trace shifts upwards if Y position control is rotated clockwise.

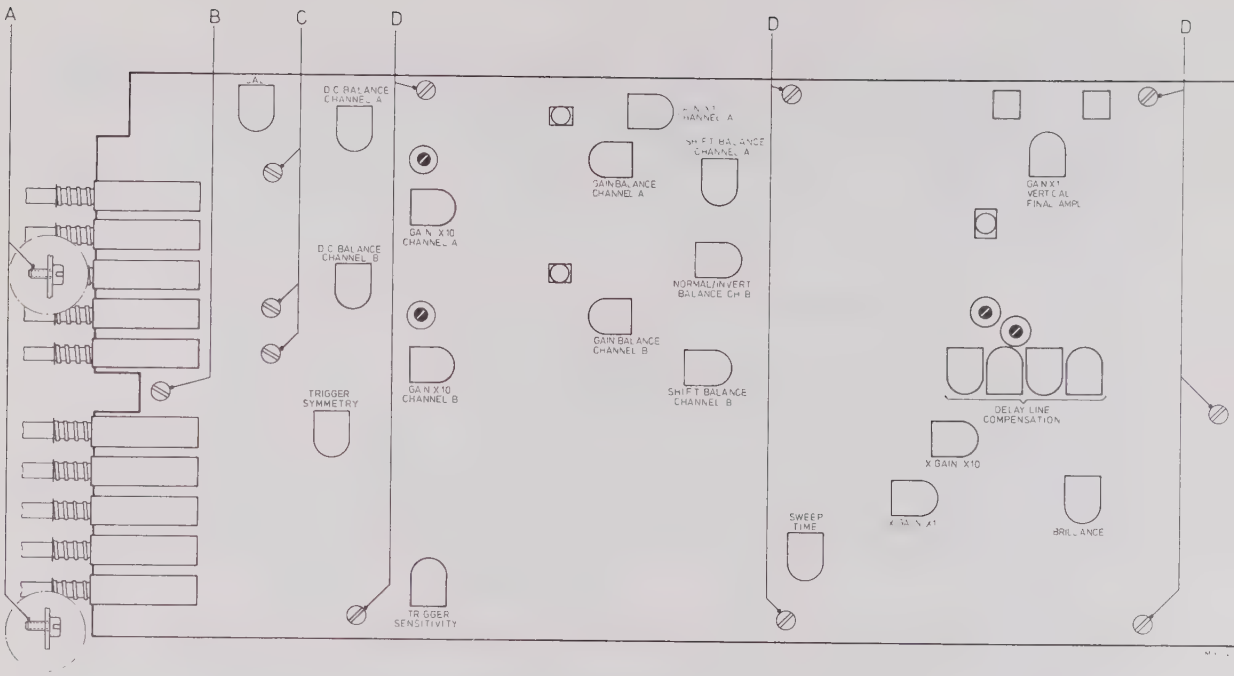


Fig.5.3. Removal of the amplifier board

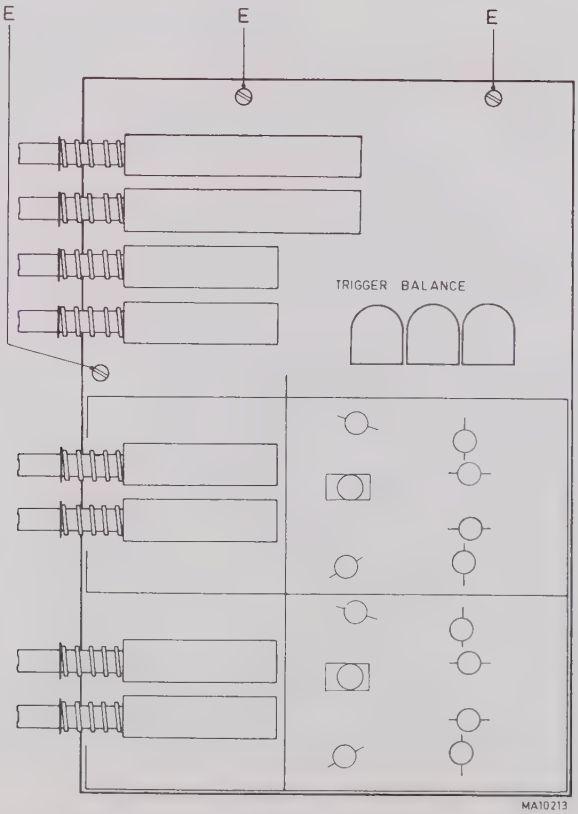


Fig.5.4. Removal of the attenuator board

5.8.Removal of the main amplifier p.c. board

- Remove covers and rear panel (section 5.2.).
- Remove the eleven retaining screws B, C and D (Fig. 5.3.).
- The main amplifier board can now be carefully lifted out of the instrument.

5.9.Replacing switches

- To replace the AMPL/DIV switches, first remove the front panel assembly (section 5.7.).
- To replace the TIME/DIV switch, first remove knobs and test plate (for this see section 5.5.).
- If one of the push-button switches of the trigger source selector (A, B, EXT, WORD) or the input coupling switch (AC/DC 0) must be replaced, it is best to remove the front panel assembly (first section 5.7.). The defective switch is then replaced in accordance with the procedure described below.
- To replace one of the push-button switches of the vertical mode switch (A, ALT, CHOP, ADD, B) or the trigger mode switch (AUTO, AC, DC, TV, SLOPE), the amplifier board (section 5.8.) can be removed if so desired and the defective switch is then replaced as described below.

5.10.A.To remove a push-button switch mounted on a p.c. board

- Remove the printed circuitboard
- Straighten the 4 retaining lugs of the relevant switch as shown in Fig. 5.5.
- Break the body of the relevant switch by means of a pair of pliers and remove the pieces. The soldering pins are then accessible.
- Remove the soldering pins and clean the holes in the printed-wiring board (e.g. with a suction soldering iron or sucking coper litze-wire).
- Solder the new switch onto the printed-circuit board.
- Bend the 4 retaining lugs back to their original positions.

Note: The ALT switch is a dummy switch which can be replaced by non-self-releasing type.

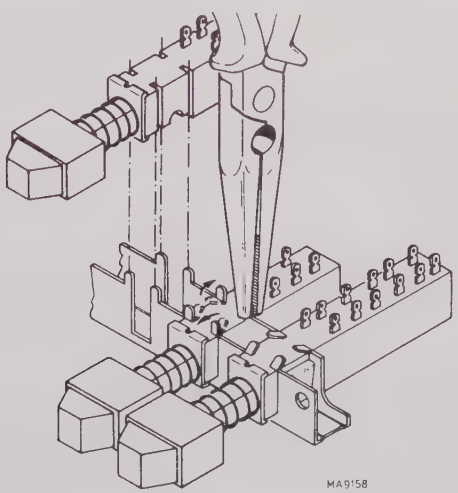


Fig.5.5. Replacing a switch-segment

5.10.B. To remove a push-button switch fitted to the front panel by means of clamping devices

- The Allen-key screws that secure the push-button set to the front panel must be removed (Fig. 5.6.).
- Straighten the 4 retaining lugs of the relevant switch as shown in Fig. 5.5.
- Remount the new switch.
- Bend the four retaining lugs back to their original positions.

Note: Before a push-button set is refitted to the front panel, it is advisable to stick the two parts of the clamping device together by means of adhesive tape or non-hardening glue, in order to facilitate replacement, refer to Fig. 5.6.

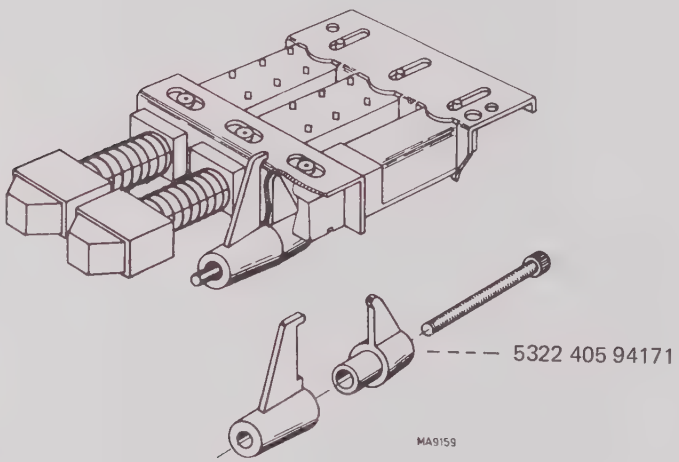


Fig.5.6. Push-button set clamping device

5.11. Removing the mains transformer

- Remove rear panel (section 5.2.).
- Remove the lid of the voltage selector compartment.
- Remove the lid of the transformer compartment.
- Lift the lid of the transformer compartment with the attached transformer at the same time sliding the cable from the voltage selector out of the slot in the transformer compartment.
- The transformer and thermal fuse are then accessible.

5.12. Replacing the thermal fuse

- Remove mains transformer (section 5.11.).
- Unsolder fuse terminals 1 and 2 (Fig. 5.7. & 5.8.).
- Only the fuse wire is replaced.
- Bend the housing of the fuse slightly outwards.
- Disengage the locking pin and pull out the wire.
- Push new fuse wire into the housing until the locking pin snaps into the hole.
- The loop in the fuse wire must point to terminal 1.
- Solder the fuse wire to terminals 1 and 2.

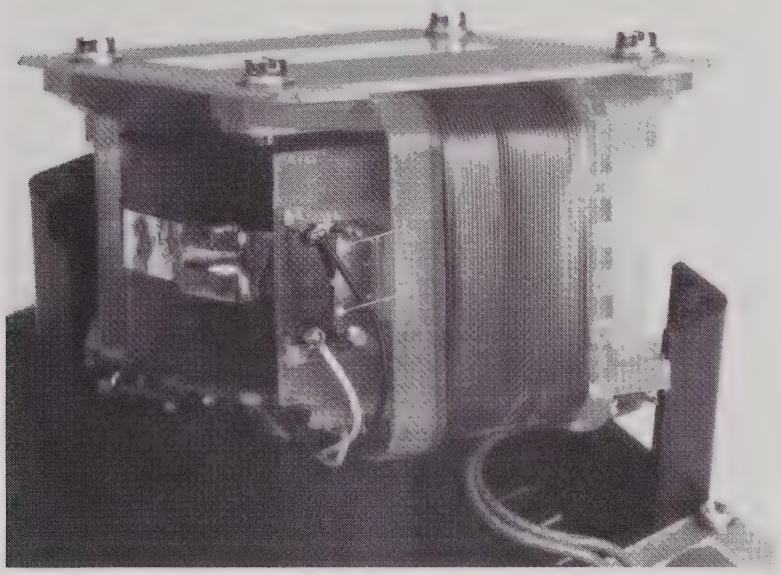


Fig.5.7. Removing the mains transformer

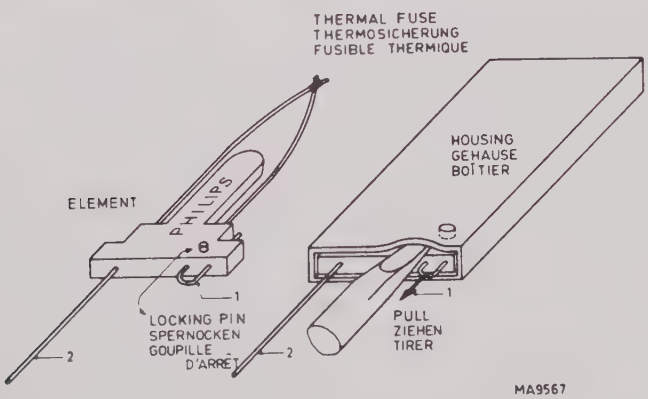


Fig.5.8. Replacing the thermal fuse

5.13. Removal of power supply printed circuit board

- Remove wrap around cover and rear panel (section 5.2.).
- Ensure connections are unplugged.
- Unfasten the two slot headed screws holding the transistor heat sinks.
- Unfasten the seven slot headed screws holding the P.C.B., the board may now be lifted out of the instrument.

5.14.Removal of the interface printed circuit board (Fig. 7.8.)

- Remove wrap around cover and rear panel (section 5.2.).
- Unplug all of the interface cables.
- Remove the three slot headed screws B, the board may now be lifted out of the instrument.

5.15.Removal of the analyzer printed circuit board (Fig. 7.4.)

- Remove wrap around cover and rear panel (section 5.2.).
- Remove connectors and leads from component side of board.
- Remove the eight screws A (Fig 7.4.).
- The board can now be removed, taking care to clear the front panel switches.
- If it is found necessary to remove the microprocessor or the E-proms great care must be taken to avoid bending the pins or breaking the encapsulation to the devices.

5.16.Removal of the printed circuit board "Options"

See Options manual.

5.17.Removal of I.C.'s soldered on p.c. board

- Cut by using a pair of cutters the soldering pins from the body of the defective I.C.
- Carefully unsolder the soldering pins of the p.c. board one after another
- Remove all superfluous soldering material. Use a sucking iron or sucking copper litze-wire.
- Check that the pin of the replacement part are clear or pre-tinned on the soldering places.
- Locate the replacement I.C. exactly on its place, and solder the new I.C. on to the p.c. board.

NOTE: Bear in mind that the maximum permissible soldering time is 10 seconds during which the temperature of the I.C. must not exceed 250 deg.C. The use of a solder with a low melting point is therefore recommended.

Take care, not to damage the plastic encapsulation of these parts during the soldering procedure (softening point of the plastic is 150 deg.C).

ATTENTION: When you are soldering inside the instrument it is essential to use a low-voltage soldering iron, the tip of which must be earthed to the mass of the instrument.

Suitable soldering irons are:
- ORYX micro-miniature soldering instrument, type 6A, voltage 6 V, in combination with PLATO pin-point tip type 0-569.
- ERSA miniature soldering iron, type minor 040 B, voltage 6 V.
- Low Voltage Mini Soldering Iron, Type 800/12 W - 6 V, power 12 W, voltage 6 V, order no. 4822 395 10004, in combination with 1 mm-pin-point tip, no. 4822 395 10012.

6. ABBREVIATIONS AND SURVEY OF THE IC´S USED

6.1. Glossery of terms and abbreviations

ADDSN		ADDress setting IEC 625 interface
CHARDY	D2122	CHARACTER READY
CKOS	D2302	CLOCK 0 SELECT
CKO	D2313/8	CLOCK 0
CK1	D2313/6	CLOCK 1
CK1SB	D2322	CLOCK 1 SELECT BUFFERED (DAM 22)
CKO1SB	D2322	CLOCK 0 OR CLOCK 1 SELECT BUFFERED
CKAC	D2371	CLOCK ADDRESS COUNTER
CKDLYC	D2371	CLOCK DELAY COUNTER
DAM	.....	DATA AQUISITION MEMORY
DAMIN	D2336	DATA AQUISITION MEMORY INPUT
DAMWR	D2336	DATA AQUISITION MEMORY WRITE
DIRDY	D2372	DATA INPUT READY
DLYZR	D2372	DELAY COUNTER ZERO
ETI	D2372	ENABLE TIMING INPUT
EDLYC	D2364	ENABLE DELAY COUNTER
ETRDLY	D2361	ENTER DELAY COUNTER
LDCHAR	D2311	LOAD CHARACTER
LDDLYH	D2301	LOAD DELAY COUNTER HIGH PART
LDDLYL	D2301	LOAD DELAY COUNTER LOW PART
LDVERT	D2311	LOAD VERTICAL
OPTRDY	X2317	OPTIONAL READY
OPTREQ	X2317	OPTIONAL REQUEST
PAR	....	PARALLEL
PCKO	D2303	POLARITY CLOCK 0
PCK1	D2303	POLARITY CLOCK 1
PODTST	X11	POD TEST
PQOCKO	D2301	POLARITY QUALIFIER 0 CLOCK 0
PQOPK1	....	POLARITY QUALIFIER 0 CLOCK 1
PQTW	D2303	POLARITY OF EXTERNAL QUALIFIER
QO,1,2	....	QUALIFIER 0, 1, 2
QPAR	....	QUASI PARALLEL
QTWIN	X5	QUALIFIER TRIGGER-WORD INPUT
QTWINS	D2377	QUALIFIER TRIGGER-WORD INPUT STORED

RESET INT	D2324(uP)	RESET INTERFACE
RESET OUT	D2324(uP)	RESET OUT (= option)
RDB	D2346	READ BUFFERED
ROW	D2359	ROW
RSYCKP	D2381	RESET SYSTEM CLOCK PULSE
RUNDI	D2301	RUN DATA INPUT
SCOL	D2321	SELECT COLOM
SCYDA	D2303	SELECT CYCLE DATA
SCYDLY	D2303	SELECT CYCLE DELAY COUNTER
SDAM	D2347	SELECT DATA AQUISITION MEMORY
SDAMAC	D2351	SELECT DATA AQUISITION MEMORY ADDRESS COUNTER
SDAMAP	D2336	SELECT DATA AQUISITION MEMORY ADDRESS POINTER
SEQ	....	SEQUENTIAL
SEQD	....	SEQUENTIAL DATA
SFALSE	SWITCH 24	SELECT FALSE MODE
SID	D2324(uP)	SERIAL INPUT DATA
SMEM	D2323	SELECT MEMORY
SMPX0	D2303	SELECT MULTIPLEX 0
SMPX1	D2303	SELECT MULTIPLEX 1
SOD	D2324(uP)	SERIAL OUTPUT DATA
SOFALSE	X 2317	SELECT OPTION FALSE
SOPTI	D2323	SELECT OPTIONAL
SPPI 1	D2347	SELECT PROGRAMMABLE PERIPHERAL INTERFACE 1
SPPI 2	D2323	SELECT PROGRAMMABLE PERIPHERAL INTERFACE 2
SQOCKO	D2303	SELECT QUALIFIER 0 CLOCK 0
SQTW (1or2)	D2303	SELECT QUALIFIER TRIGGER-WORD 1 OR 2
SRAM	D2334	SELECT RAM
SROM	D2323	SELECT ROM
STRDI	D2311	START DATA INPUT
STWCKO	D2303	SELECT TRIGGER-WORD CLOCK 0
STWM	D2347	SELECT TRIGGER-WORD MEMORY
SWL FALSE	X2301	SWITCH LINE FALSE
SYCKP	D2314/8	SYSTEM CLOCK PULSE
TW 2	D2362	TRIGGER-WORD 2
TWCKO	D2362 (D2322)	TRIGGER-WORD CLOCK 0 (DAM 21)
TWIN	X10	TRIGGER-WORD INPUT
TWINS	D2377	TRIGGER-WORD INPUT STORED
TWMWR	D2336	TRIGGER-WORD MEMORY WRITE/READ
TWOUT	D2309....	TRIGGER-WORD OUT
VADIB	D2322	VALID DATA INPUT BUFFERED
WRB	D2346	WRITE BUFFERED

6.2. LIST OF I.C's USED

Nr.	TYPE	ADDITIONAL INFORMATION	SUPPLIER
1	N 74 S 00 N	Quad 2-input NAND gate	Signetics
2	N 74 S 04 N	Inverter (6x)	Signetics
3	N 74 LS 05 N	Inverter (6x) open collector	Signetics
4	N 74 LS 08 N	Quad 2-input AND gate	Signetics
5	N 74 S 10 N	Triple 3-input NAND gate	Signetics
6	N 74 LS 21 N	Dual 4-input AND gate	Signetics
7	N 74 LS 32 N	Quad 2-input OR gate	Signetics, Texas instr.
8	SN 74 S 74 N-00	D-posit edge triggered F.F.(2x)	Signetics
9	N 74 S 86 N	Quad 2-input EX-OR gate	Signetics
10	SN 74 LS 123 N-00	Retrigg. monostab. multivibr. (2x)	Signetics, Texas instr.
11	74 LS 132	Quad 2-input NAND Schmitt. Trigger	Signetics
12	N 74 LS 138 N	1 of 8 decoder/demax.	Signetics
13	SN 74 LS 151 N-00	8 to 1 mux/data selector	Signetics, Texas instr.
14	N 74 S 153 N	Dual 4 to 1 multiplexer	Signetics
15	N 74 LS 154 N	1 of 16 decoder/demuxate	Signetics
16	N 74 LS 156 N	Dual 2 to 4 decoder/demux open collec.	Signetics
17	N 74 LS 191 N	Binary up/down counter	Signetics
18	SN 74 LS 240 N-00	Oct. inverting buffers (3-state)	Signetics
19	SN 74 LS 244 N	Oct. buffers (3-state)	Signetics, Texas instr.
20	SN 74 LS 257 N	Quad 2 to 1 mux/data selector	Signetics, Texas instr.
21	SN 74 LS 279 N	Quad s - r latch	Signetics, Texas instr.
22	SN 74 LS 373 N	Oct. transparent latch (3-state)	Signetics, Texas instr.
23	SN 74 LS 374 N	Oct. D. posit edge triggered F.F. (3-state)	Signetics, Texas instr.
24	N 82 S 117 N	256 x 1-bit biplar RAM	Signetics
25	AM 9124 CPC	1024 x 4-bit RAM	AM
26	HEF 4029 BP	Counter up/down, bin/dec.	Philips, Sign.
27	HEF 4042 BP	D-latch (4x)	Philips
28	HEF 4050 BP	Non-inverting buffers (6x)	Philips
29	HEF 40174 BP	D-latch (6x)	Philips
30	LM 311 N	Analog voltage comparator	Signetics
31	LF 357 N	J-Fet Opamp	Motorola, Philips
32	NE 522 N	Comparator/Sense apml.	Signetics
33	NE 5008 N	8-bit D.A. converter	Signetics
34	P 8255 A	Progr. peripheral interface	Intel
35	2716	EPROM (charac. generator)	Intel, Signetics
36	2732	EPROM 4k x 8 (PROM set programmed)	Intel
37	P 8085 A	Microprocessor	Intel
38	93422 PC	256 x 4-bit RAM	Fairchild

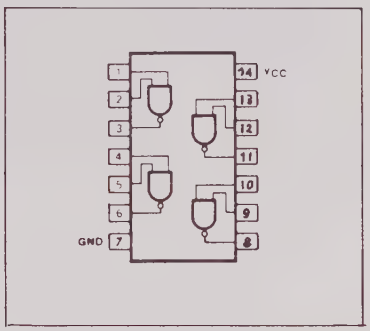
6.3. TRUTH TABLES AND PIN CONFIGURATION OF IC´S USEDED

QUAD 2-INPUT NAND GATE — 74 SERIES "00"

TRUTH TABLE

A	B	X
0	0	1
1	0	1
0	1	1
1	1	0

PIN CONFIGURATIONS

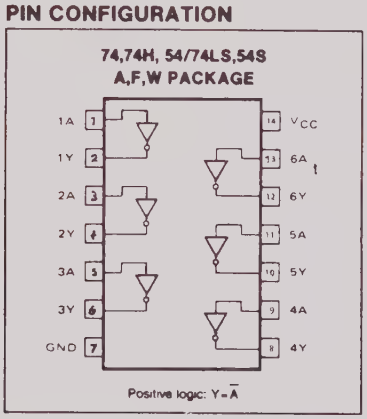


HEX INVERTER — 7404

TRUTH TABLE

A	Y
0	1
1	0

PIN CONFIGURATION

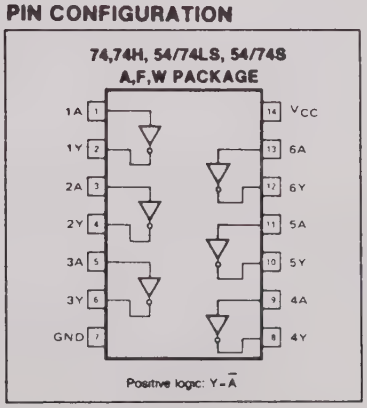


HEX INVERTER W/OPEN COLLECTOR OUTPUTS — 54/7405

TRUTH TABLE

A	Y
0	1
1	0

PIN CONFIGURATION

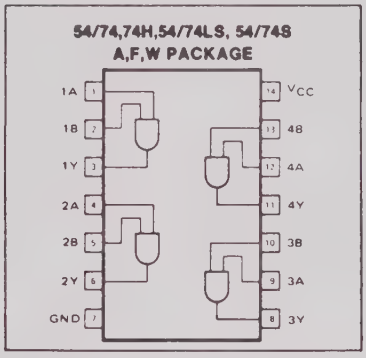


QUAD 2-INPUT AND GATE — 7408

TRUTH TABLE

A	B	X
0	0	0
1	0	0
0	1	0
1	1	1

PIN CONFIGURATION

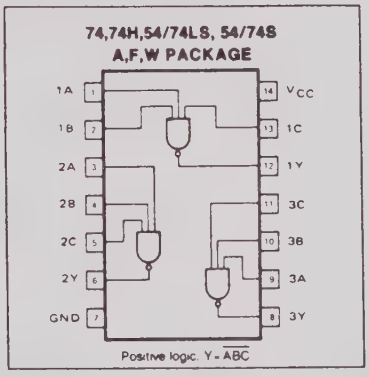


TRIPLE 3-INPUT NAND GATE — 54/7410

TRUTH TABLE

A	B	C	Y
0	0	0	1
1	0	0	0
1	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	0

PIN CONFIGURATION

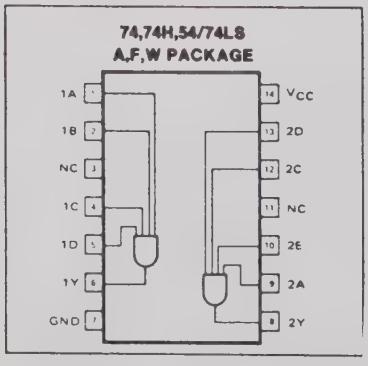


DUAL 4-INPUT AND GATE — 54/7421

TRUTH TABLE

A	B	C	D	X
0	0	0	0	0
1	0	0	0	0
0	1	0	0	0
1	1	0	0	0
0	0	1	0	0
1	0	1	0	0
0	1	1	0	0
1	1	1	0	0
0	0	0	1	0
1	0	0	1	0
0	1	0	1	0
1	1	0	1	0
0	0	1	1	0
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1

PIN CONFIGURATION

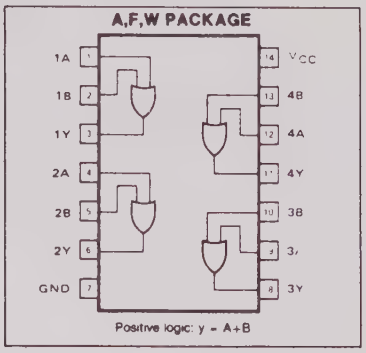


QUAD 2-INPUT OR GATE — 54/7432

TRUTH TABLE

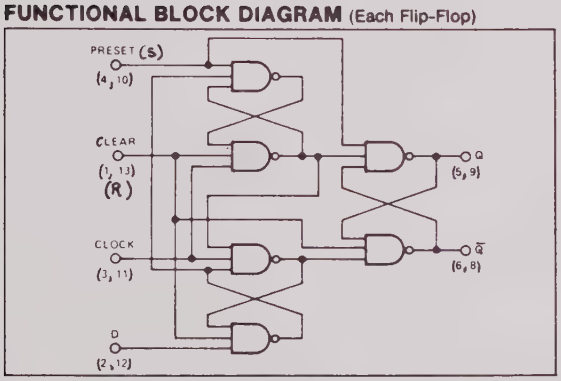
A	B	X
0	0	0
1	0	1
0	1	1
1	1	1

PIN CONFIGURATION

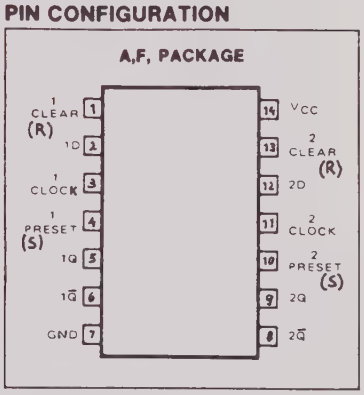


DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOP — 7474

FUNCTIONAL BLOCK DIAGRAM (Each Flip-Flop)



PIN CONFIGURATION



DESCRIPTION

Preset and clear inputs are active-low and operate independently of the clock input. When preset and clear are inactive (high), information at the D input is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D-input signal has no effect at the output.

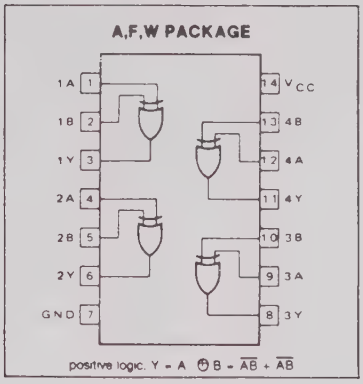
TRUTH TABLE (Each Flip-Flop)

	Inputs			Outputs	
Preset ($\overline{S}$)	Clear ($\overline{R}$)	Clock	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = high level (steady state) L = low level (steady state)
*This condition is nonstable. It will not remain after clear and preset return to their inactive (high) state.

QUAD 2-INPUT EXCLUSIVE-OR GATE 7486

PIN CONFIGURATION



FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = high level, L = low level

DUAL RETRIGGERABLE MONOSTABLE MULTIVRIBRATOR 54/74 SERIES "123"

DESCRIPTION

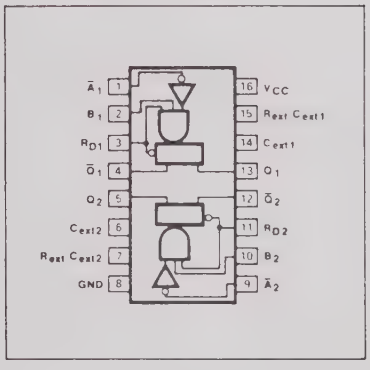
These retriggerable monostable multivibrators feature dc triggering from gated active LOW inputs ($\overline{A}$) and active HIGH inputs (B) and also provide overriding direct reset inputs. Complementary outputs are provided. The retrigger capability simplifies the generation of output pulses of extremely long duration. By triggering the input before the output pulse is terminated, the output pulse may be extended. The overriding reset capability permits any output pulse to be terminated at a predetermined time independently of the timing components R and C.

FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{R}_D$	$\overline{A}$	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⊓	⊔
H	↓	H	⊓	⊔
↑	L	H	⊓	⊔

H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW-to-HIGH transition
↓ = HIGH-to-LOW transition

PIN CONFIGURATIONS



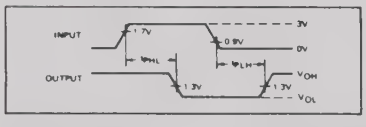
QUAD 2-INPUT NAND SCHMITT TRIGGER 54/74132

DESCRIPTION

Each circuit functions as a NAND gate, but because of the Schmitt action, it has different input threshold levels for positive- and negative-going signals. The hysteresis or backlash, which is the difference between the two threshold levels, is typically 800 millivolts.

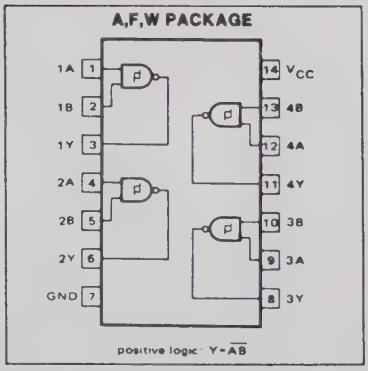
These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean, jitter-free output signals.

PARAMETER MEASUREMENT INFORMATION



NOTES:
A. The input waveform is supplied by a generator with the following characteristics. Z_{out} = 50 Ω and PRR ≤ 1 MHz, t_r ≤ 15 ns, t_f ≤ 6 ns.

PIN CONFIGURATION



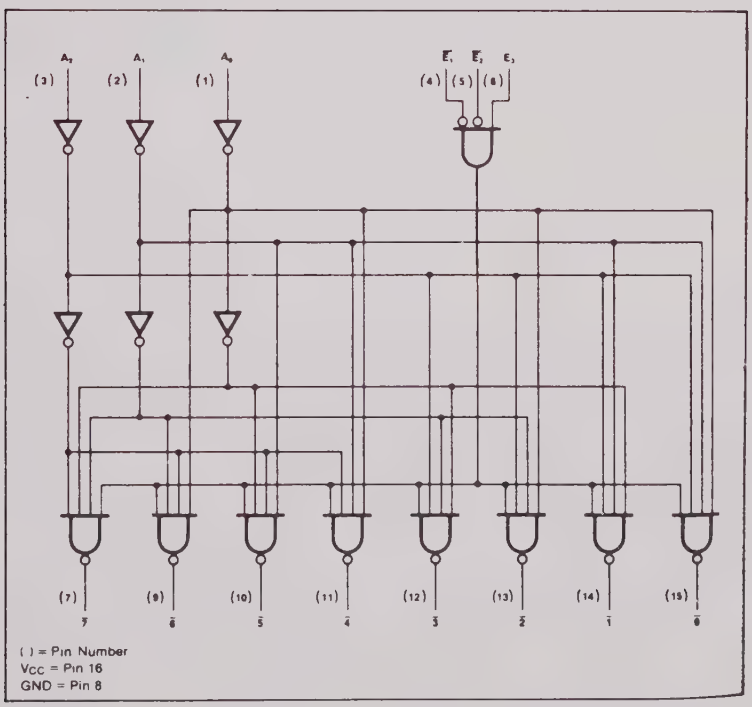
TRUTH TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

NOTES

H = HIGH voltage level
L = LOW voltage level
X = Don't care

LOGIC DIAGRAM



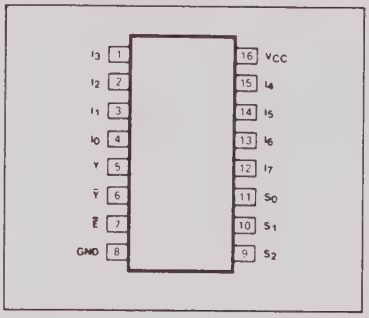
( ) = Pin Number
V_{CC} = Pin 16
GND = Pin 8

8-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER 74151

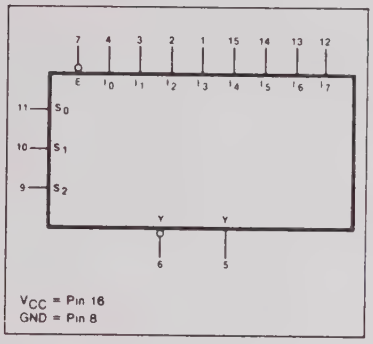
DESCRIPTION

The "151" is a high speed 8-input multiplexer providing, in one package, the ability to select one bit of data from up to eight sources. The device can be used as a universal function generator to generate any logic function of four variables.

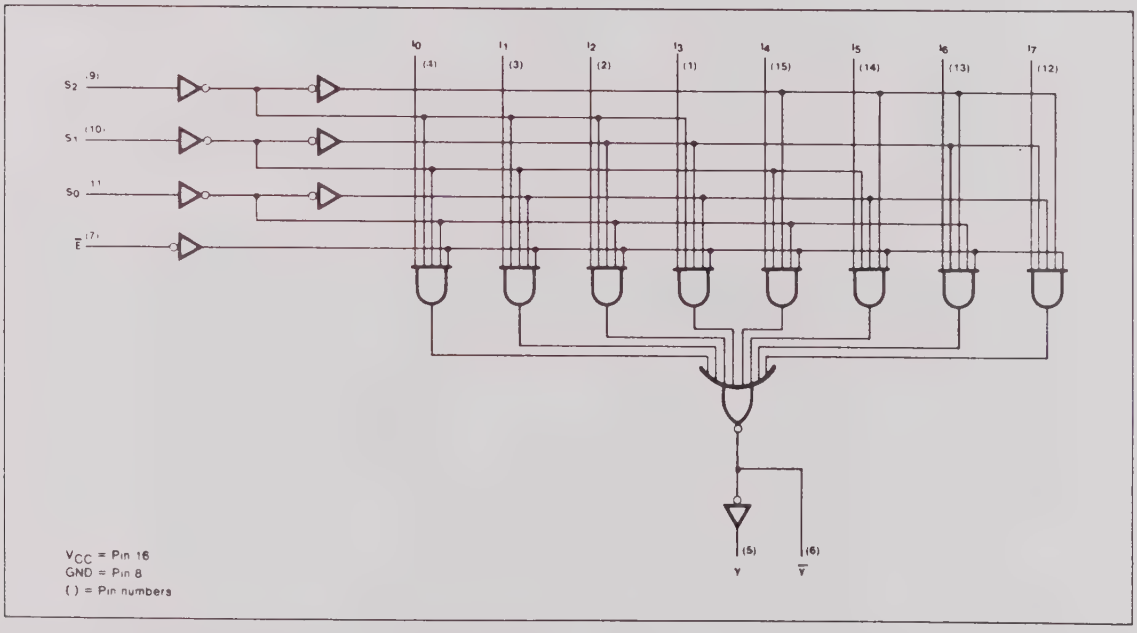
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The "151" is a logical implementation of a single pole, 8-position switch with the switch position controlled by the state of three select inputs, S_0, S_1, S_2. True (Y) and complement ($\overline{Y}$) outputs are both provided. The Enable input ($\overline{E}$) is active LOW. When $\overline{E}$ is HIGH the $\overline{Y}$ output is HIGH and the Y output is LOW regardless of all other inputs. The logic function provided at the output is:

$$Y = \overline{E} \cdot (I_0 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_1 \cdot S_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_2 \cdot \overline{S}_0 \cdot S_1 \cdot \overline{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S}_2 + I_4 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S}_1 \cdot S_2 + I_6 \cdot \overline{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2).$$

In one package the "151" provides the ability to select from eight sources of data or control information. The device can provide any logic function of four variables and its negation with correct manipulation.

TRUTH TABLES

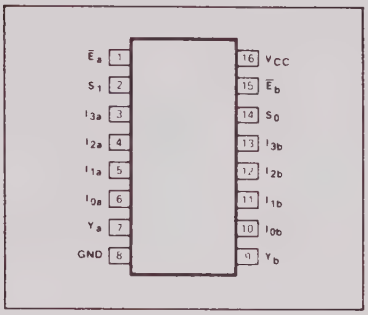
INPUTS												OUTPUTS	
$\overline{E}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Y}$	Y
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH Voltage level
L = LOW Voltage level
X = Don't care

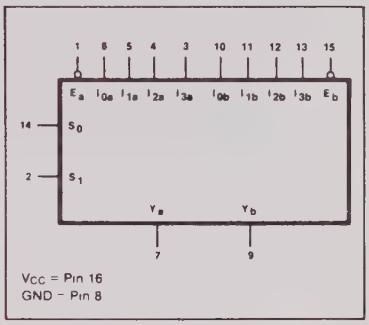
DESCRIPTION

The "153" is a high speed Dual 4-Input Multiplexer with common Select inputs and individual Enable inputs for each section. The device can select two bits of data from four sources. The two buffered outputs present data in the non-inverted (true) form. The "153" can generate any two functions of three variables in addition to multiplexer operation.

PIN CONFIGURATION



LOGIC SYMBOL



FUNCTIONAL DESCRIPTION

The "153" is a Dual 4-input Multiplexer that can select two bits of data from up to four sources under control of the common Select inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active LOW Enables ($\overline{E}_a$, $\overline{E}_b$) which can be used to strobe the outputs independently. Outputs (Y_a, Y_b) are forced LOW when the corresponding Enables ($\overline{E}_a$, $\overline{E}_b$) are HIGH.

The device is the logical implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select inputs. The logic equations for the outputs are shown below.

$$Y_a = \overline{E}_a \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0)$$

$$Y_b = \overline{E}_b \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0)$$

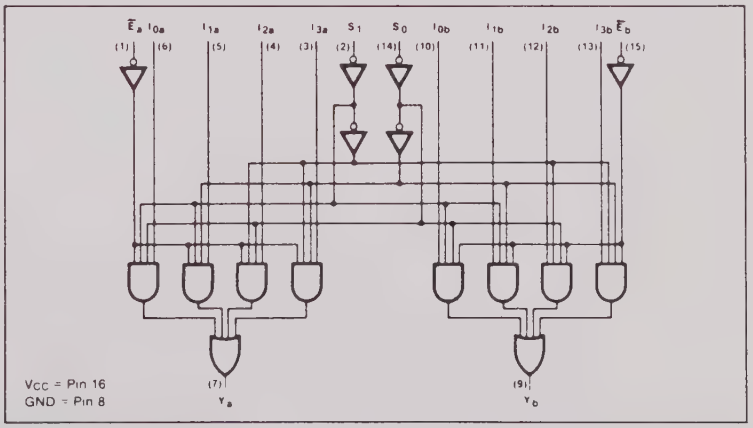
The "153" can be used to move data to a common output bus from a group of registers. The state of the Select inputs would determine the particular register from which the data came. An alternative application is as a function generator. The device can generate two functions of three variables This is useful for implementing highly irregular random logic.

TRUTH TABLE

SELECT INPUTS		INPUTS (a or b)					OUTPUT
S_0	S_1	$\overline{E}$	I_0	I_1	I_2	I_3	Y
X	X	H	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	L
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care

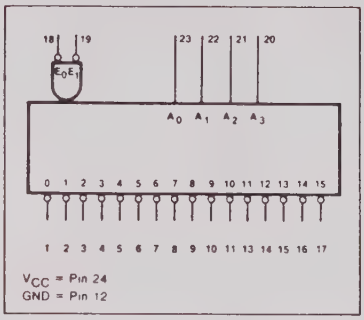
LOGIC DIAGRAM



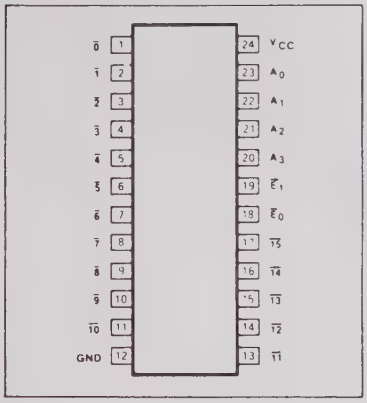
DESCRIPTION

The "154" is a 4-line to 16-line Decoder/Demultiplexer with a 2-input enable gate. It is designed to accept 4-bits of binary data and provide 1-of-16 mutually exclusive active LOW outputs. The enable can be used as a data input to demultiplex up to 16-bits of serial data.

LOGIC SYMBOL



PIN CONFIGURATION



FUNCTIONAL DESCRIPTION

The "154" decoder accepts four active HIGH binary address inputs and provides 16 mutually exclusive active LOW outputs. The 2-input enable gate can be used to strobe the decoder to eliminate the normal decoding "glitches" on the outputs, or it can be used for expansion of the decoder. The enable gate has two AND'ed inputs which must be LOW to enable the outputs.

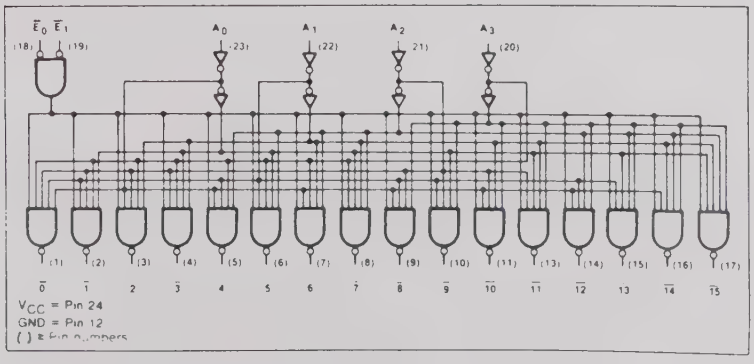
The "154" can be used as a 1-of-16 demultiplexer by using one of the enable inputs as the multiplexed data input. When the other enable is LOW, the addressed output will follow the state of the applied data.

TRUTH TABLE

INPUTS						OUTPUTS															
$\overline{E}_0$	$\overline{E}_1$	A_3	A_2	A_1	A_0	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$	$\overline{10}$	$\overline{11}$	$\overline{12}$	$\overline{13}$	$\overline{14}$	$\overline{15}$
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

LOGIC DIAGRAM

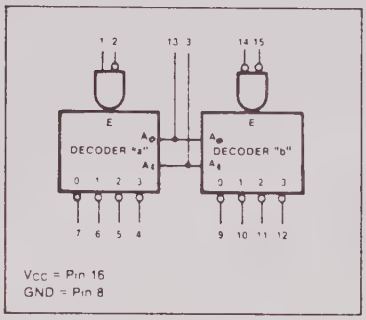

$\overline{E}_0$ $\overline{E}_1$
(18) (19)
A_0 (23)
A_1 (22)
A_2 21)
A_3 (20)
(1) (2) (3) (4) (5) (6) (7) (8) (9) (10) (11) (13) (14) (15) (16) (17)
$\overline{0}$ $\overline{1}$ 2 $\overline{3}$ 4 5 6 $\overline{7}$ $\overline{8}$ $\overline{9}$ $\overline{10}$ $\overline{11}$ $\overline{12}$ 13 $\overline{14}$ $\overline{15}$
V_{CC} = Pin 24
GND = Pin 12
( ) = Pin numbers

DUAL 2-LINE to 4-LINE DECODER/DEMULTIPLEXER (OPEN COLLECTOR) 54/74 SERIES "156"

DESCRIPTION

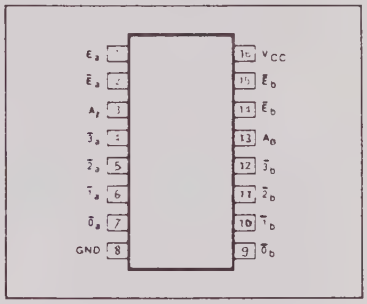
The "156" is a high speed Dual 1-of-4 Decoder/Demultiplexer with open collector outputs featuring common binary-address inputs and separate gated Enable inputs. Decoder "a" has an Enable gate with one active HIGH and one active LOW input. Decoder "b" has two active LOW Enable inputs. If the Enable functions are satisfied, one output of each decoder will be LOW as selected by the address inputs. Wired-OR (Dot-AND) decoding and function generator applications are available through the open collector outputs of the "156."

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

PIN CONFIGURATION



FUNCTIONAL DESCRIPTION

The "156" is a Dual 1-of-4 Decoder/Demultiplexer with common Address inputs and gated Enable inputs. Each decoder section, when enabled, will accept the binary weighted Address inputs (A_0,A_1) and provide four mutually exclusive active LOW outputs ($\overline{0}$-$\overline{3}$). When the Enable requirements of each decoder are not met, all outputs of that decoder are HIGH.

Both decoder sections have a 2-input enable gate. For Decoder "a" the enable gate requires one active HIGH input and one active LOW input ($E_a \cdot \overline{E}_a$). Decoder "a" can accept either true or complemented data in demultiplexing applications, by using the $\overline{E}_a$ or E_a inputs respectively. The Decoder "b" enable gate requires two active LOW inputs ($\overline{E}_b \cdot \overline{E}_b$). The device can be used as a 1-of-8 Decoder/Demultiplexer by tying E_a to $\overline{E}_b$ and relabeling the common connection address as (A_2); forming the common enable by connecting the remaining $\overline{E}_b$ and $\overline{E}_a$.

The "156" can be used to generate all 4 minterms of 2 variables. The 4 minterms are useful to replace multiple gate functions in some applications. A further advantage of the "156" is being able to AND the minterm functions by tying outputs together. Any number of terms can be wired-AND as shown in the formula below.

$$f = (E + A_0 + A_1) \cdot (E + \overline{A}_0 + A_1) \cdot (E + A_0 + \overline{A}_1) \cdot (E + \overline{A}_0 + \overline{A}_1)$$

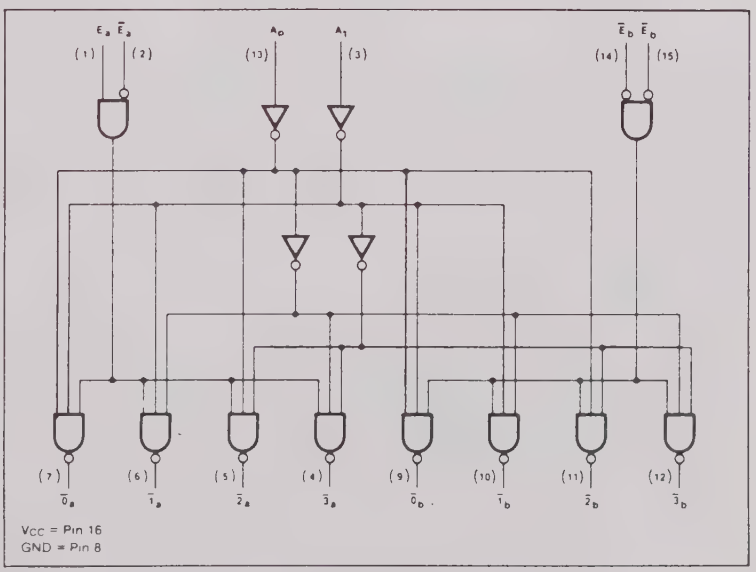
where $E = E_a + E_a$, $E = E_b + E_b$

TRUTH TABLE

ADDRESS		ENABLE "a"		OUTPUT "a"				ENABLE "b"		OUTPUT "b"			
A_0	A_1	E_a	$\overline{E}_a$	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{E}_b$	$\overline{E}_b$	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$
X	X	L	X	H	H	H	H	H	X	H	H	H	H
X	X	X	H	H	H	H	H	X	H	H	H	H	H
L	L	H	L	L	H	H	H	L	L	L	H	H	H
H	L	H	L	H	L	H	H	L	L	H	L	H	H
L	H	H	L	H	H	L	H	L	L	H	H	L	H
H	H	H	L	H	H	H	L	L	L	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

LOGIC DIAGRAM



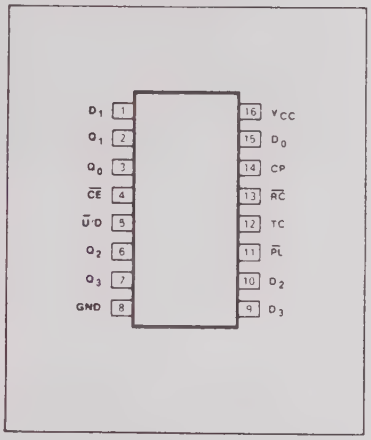
V_{CC} = Pin 16
GND = Pin 8

54/74191
54LS/74LS191

FEATURES

- **Synchronous, reversible 4-bit binary counting**
- **Asynchronous parallel load capability**
- **Count Enable control for synchronous expansion**
- **Single Up/Down control input**

PIN CONFIGURATION

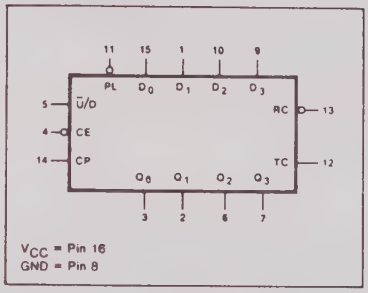


DESCRIPTION

The "191" is a presettable 4-Bit Binary Up/Down Counter with state changes of the counter synchronous with the LOW-to-HIGH transition of the Clock Pulse input.

The circuit features an asynchronous Parallel Load ($\overline{PL}$) input which overrides counting and loads the data present on the D_n inputs into the flip-flops. Synchronous expansion in a multistage counter is made possible by a Count Enable ($\overline{CE}$) input. The count up or count down mode is determined by an Up/Down ($\overline{U}/D$) input. A variety of methods for generating carry/borrow signals in multistage counter application is made possible by Terminal Count (TC) and Ripple Clock ($\overline{RC}$) outputs.

LOGIC SYMBOL



FUNCTIONAL DESCRIPTION

The "191" is an asynchronously presettable Up/Down 4-Bit Binary Counter. It contains four master/slave flip-flops with internal gating and steering logic to provide asynchronous preset and synchronous count-up and count-down operation.

Asynchronous parallel load capability permits the counter to be preset to any desired number. Information present on the parallel Data inputs (D_0-D_3) is loaded into the counter and appears on the outputs when the Parallel Load ($\overline{PL}$) input is LOW. As indicated in the Mode Select Table, this operation overrides the counting function.

Counting is inhibited by a HIGH level on the Count Enable ($\overline{CE}$) input. When $\overline{CE}$ is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the Clock input. The Up/Down ($\overline{U}/D$) input signal determines the direction of counting as indicated in the Mode Select Table. The $\overline{CE}$ input may go LOW when the clock is in either state, however, the LOW-to-HIGH $\overline{CE}$ transition must occur only while the Clock is HIGH. Also, the $\overline{U}/D$ input should be changed only when either $\overline{CE}$ or CP is HIGH.

MODE SELECT-FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS
	$\overline{PL}$	$\overline{U}/D$	$\overline{CE}$	CP	D_n	Q_n
Parallel load	L	X	X	X	L	L
	L	X	X	X	H	H
Count up	H	L	l	↑	X	count up
Count down	H	H	l	↑	X	count down
Hold "do nothing"	H	X	H	X	X	no change

TC AND $\overline{RC}$ TRUTH TABLE

INPUTS			TERMINAL COUNT STATE				OUTPUTS	
$\overline{U}/D$	$\overline{CE}$	CP	Q_0	Q_1	Q_2	Q_3	TC	$\overline{RC}$
H	X	X	H	H	H	H	L	H
L	H	X	H	H	H	H	H	H
L	L	⊔	H	H	H	H	H	⊔
L	X	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⊔	L	L	L	L	H	⊔

H = HIGH voltage level steady state
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
X = Don't care.
↑ = LOW-to-HIGH clock transition.
⊔ = LOW pulse.

OCTAL INVERTER BUFFER (3-STATE) — 54/74 SERIES "240"

PIN CONFIGURATION

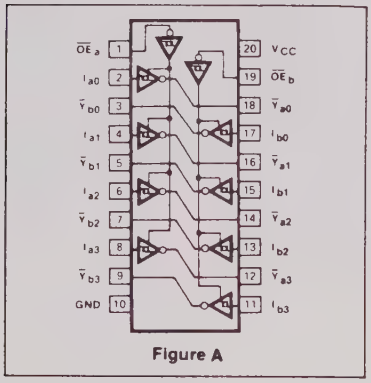


Figure A

TRUTH TABLE

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	$\overline{OE}_b$	I_b	$\overline{Y}_a$	$\overline{Y}_b$
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	(Z)	(Z)

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = High impedance (off) state

OCTAL BUFFERS (3-STATE) — 54/74 SERIES "244"

PIN CONFIGURATION

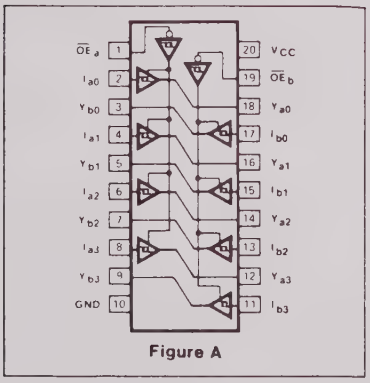


Figure A

TRUTH TABLE

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	$\overline{OE}_b$	I_b	Y_a	Y_b
L	L	L	L	L	L
L	H	L	H	H	H
H	X	H	X	(Z)	(Z)

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = High impedance (off) state

QUAD SET–RESET LATCH — 54/74 SERIES "279"

PIN CONFIGURATION

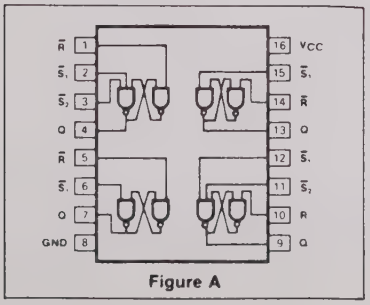


Figure A

TRUTH TABLE

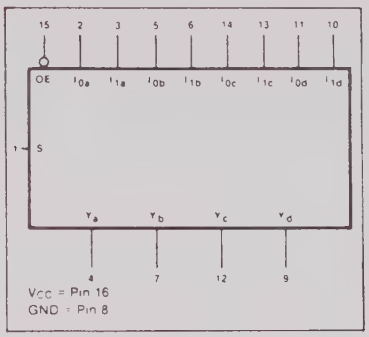
INPUTS			OUTPUT
$\overline{S}_1$	$\overline{S}_2$	$\overline{R}$	Q
L	L	L	h
L	X	H	H
X	L	H	H
H	H	L	L
H	H	H	No change

L = LOW voltage level
H = HIGH voltage level
X = Don't care
h = The output is HIGH as long as S_1 or S_2 is LOW. If all inputs go HIGH simultaneously, the output state is indeterminate, otherwise it follows the truth table

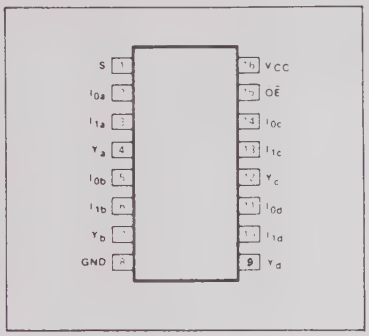
DESCRIPTION

The Quad 2-Input Multiplexer with 3-State outputs can select four bits of data from two sources using a common Data Select input. The four outputs of the "257" present data in true (non-inverted) form. The outputs may be set to a high impedance state with a HIGH on the common Output Enable ($\overline{OE}$) input allowing the outputs to interface directly with 3-State bus-organized systems.

LOGIC SYMBOL



PIN CONFIGURATION



FUNCTIONAL DESCRIPTION

The "257" has four identical 2-Input Multiplexers with 3-State outputs which select four bits of data from two sources under control of a common Data Select Input (S). The I_0 inputs are selected when the Select Input is LOW and the I_1 inputs are selected when the Select Input is HIGH. Data appears at the outputs in true (non-inverted) form from the selected inputs.

The "257" is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select Input.

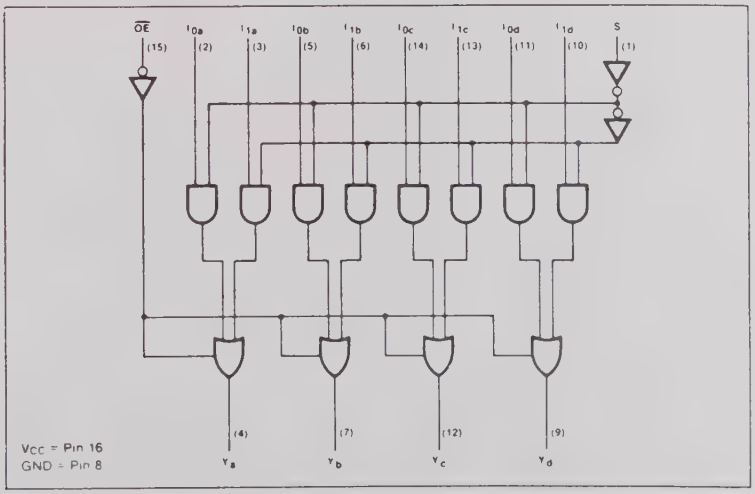
Outputs are forced to a high impedance "off" state when the Output Enable Input ($\overline{OE}$) is HIGH. All but one device must be in the high impedance state to avoid currents exceeding the maximum ratings if outputs are tied together. Design of the Output Enable signals must ensure that there is no overlap when outputs of 3-State devices are tied together.

TRUTH TABLE

ENABLE	SELECT INPUT	INPUTS		OUTPUT
$\overline{OE}$	S	I_0	I_1	Y
H	X	X	X	(Z)
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = High impedance (off) state

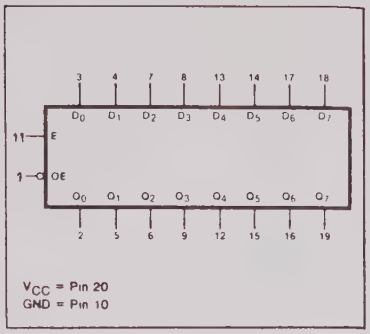
LOGIC DIAGRAM



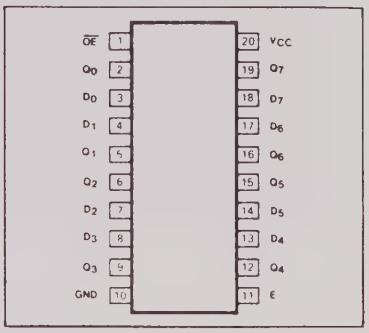
DESCRIPTION

The "373" is an 8-Bit Transparent Latch with 3-state buffered outputs. The latch outputs follow the data inputs when the latch Enable is HIGH, and they are stable when the Enable is LOW. The 3-state output buffers are controlled by an active LOW Output Enable ($\overline{OE}$) input. A HIGH on the $\overline{OE}$ input forces the eight outputs to the high impedance "off" state. When $\overline{OE}$ is LOW, the latched or transparent data appears at the outputs.

LOGIC SYMBOL



PIN CONFIGURATION



FUNCTIONAL DESCRIPTION

The "373" is Octal Transparent Latch coupled to eight 3-state output buffers. The two sections of the device are controlled independently by Latch Enable (E) and Output Enable ($\overline{OE}$) control gates.

The data on the D inputs transferred to the latch outputs when the Latch Enable (E) input is HIGH. The latch remains transparent to the data inputs while E is HIGH, and stores the data present one setup time before the HIGH-to-LOW enable transition. The enable gate has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause on the latching operation.

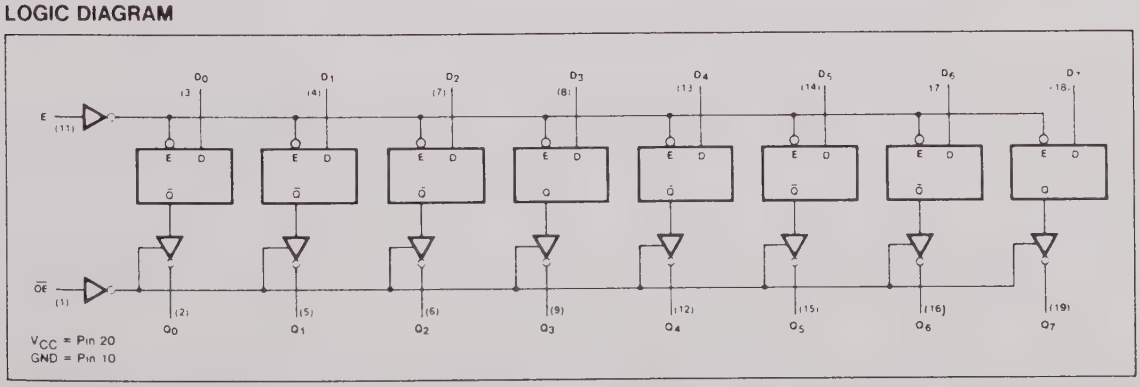
The 3-state output buffers are designed to drive heavily loaded 3-state buses, MOS memories, or MOS microprocessors. The active LOW Output Enable ($\overline{OE}$) controls all eight 3-state buffers independent of the latch operation. When $\overline{OE}$ is LOW, the latched or transparent data appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the high impedance "off" state, which means they will neither drive nor load the bus.

MODE SELECT—FUNCTION TABLE

OPERATING MODES	INPUTS				OUTPUTS
	$\overline{OE}$	E	D_n	INTERNAL REGISTER	Q_0-Q_7
Enable & read register	L L	H H	L H	L H	L H
Latch & read register	L L	L L	l h	L H	L H
Latch register & disable outputs	H H	L L	l h	L H	(Z) (Z)

H = HIGH voltagel level
h = HIGH voltage one setup time prior to the HIGH-to-LOW enable transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the HIGH-to-LOW enable transition
(Z) = High impedance "off" state

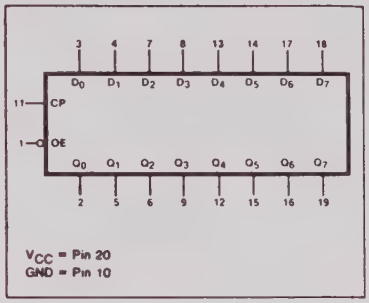
LOGIC DIAGRAM



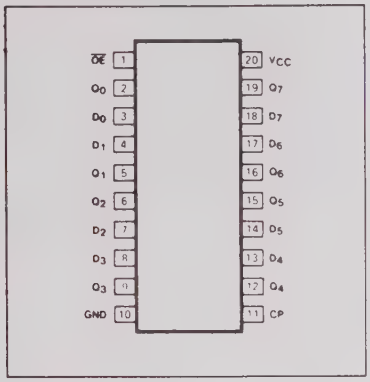
DESCRIPTION

The "374" is an Octal D Flip-Flop with 3-State buffered outputs. The device is used primarily as an 8-bit positive edge triggered storage register for interfacing with a 3-State bus. Data on the D inputs is transferred to storage during the LOW-to-HIGH transition of the Clock (CP) input. The 3-State output buffers are controlled by an active LOW Output Enable ($\overline{OE}$) input. A HIGH on the $\overline{OE}$ input forces the eight outputs to the high impedance "off" state. When $\overline{OE}$ is LOW, the data in the register appears at the outputs.

LOGIC SYMBOL



PIN CONFIGURATION



FUNCTIONAL DESCRIPTION

The "374" is an 8-bit edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable ($\overline{OE}$) control gates.

The register is fully edge triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The clock buffer has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause on the clocking operation.

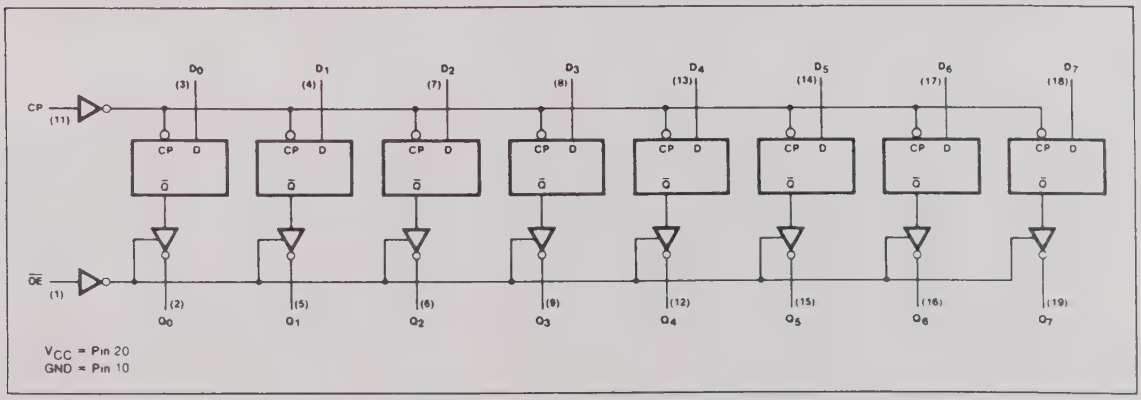
The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active LOW Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the register operation. When $\overline{OE}$ is LOW, the data in the register appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the high impedance "off" state, which means they will neither drive nor load the bus.

MODE SELECT—FUNCTION TABLE

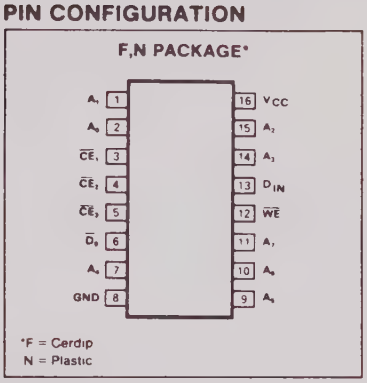
OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	CP	D_n		Q_0-Q_7
Load & read register	L	↑	l	L	L
	L	↑	h	H	H
Load register & disable outputs	H	↑	l	L	(Z)
	H	↑	h	H	(Z)

H = HIGH voltage level
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
(Z) = HIGH impedance "off" state
↑ = LOW-to-HIGH clock transition

LOGIC DIAGRAM



PIN CONFIGURATION

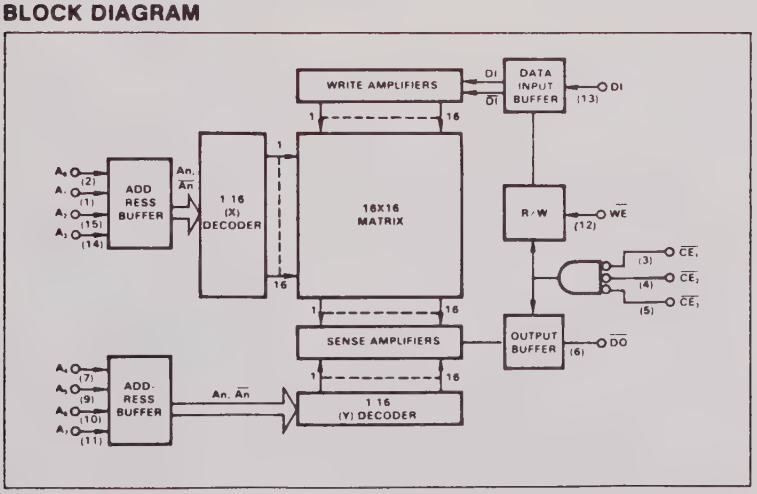


TRUTH TABLE

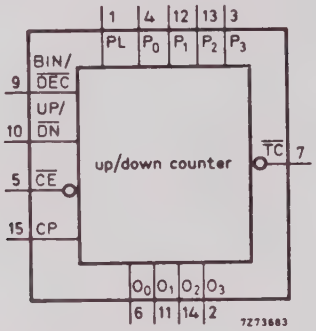
MODE	$\overline{CE}$*	$\overline{WE}$	D_{IN}	$\overline{D}_{OUT}$	
				82S16/116	82S17/117
Read	0	1	X	Stored $\overline{data}$	Stored $\overline{data}$
Write "0"	0	0	0	1	1
Write "1"	0	0	1	0	0
Diasabled	1	X	X	High-Z	1

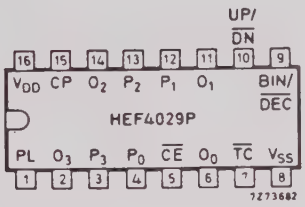
*"0" = All $\overline{CE}$ inputs low; "1" = one or more $\overline{CE}$ inputs high
X = Don't care.

BLOCK DIAGRAM



DUAL 4-INPUT AND GATE — HEF4029P





GENERAL DESCRIPTION

The HEF4029P is a synchronous edge-triggered up/down 4-bit binary/BCD decade counter with a clock input (CP), an active LOW count enable input ($\overline{CE}$), an up/down control input (UP/$\overline{DN}$), a binary/decade control input (BIN/$\overline{DEC}$), an overriding asynchronous active HIGH parallel load input (PL), four parallel data inputs (P_0 to P_3), four parallel buffered outputs (O_0 to O_3) and an active LOW terminal count output ($\overline{TC}$).

Information on P_0 to P_3 is loaded into the counter while PL is HIGH, independent of all other input conditions. With PL LOW, operation is synchronous and is edge-triggered on the LOW-to-HIGH transition of CP. Operation is determined by the three synchronous mode control inputs; UP/$\overline{DN}$, BIN/$\overline{DEC}$ and $\overline{CE}$.
These inputs must be stable only during the set-up time prior to the LOW-to-HIGH transition of CP and the hold time after this clock transition.
$\overline{TC}$ is LOW when the counter is at its terminal count, as determined by the counting mode, and $\overline{CE}$ is LOW.

QUADRUPLE D–LATCH — HEF4042B

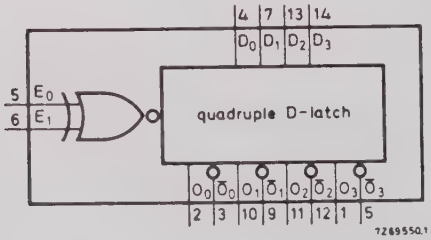
The HE family of LOCMOS (Local Oxidation Complementary MOS) is designed for medium-speed digital equipment in computation, telecommunication, instrumentation and control.
Recommended supply voltage range 3 to 15 V.
Inputs and outputs are protected against electrostatic effects in a wide variety of device-handling situations. However, to be totally safe, it is desirable to take handling precautions into account.

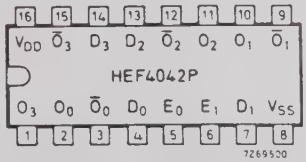
PINNING

D_0 to D_3	data inputs
E_0 and E_1	enable inputs
O_0 to O_3	parallel latch outputs
$\overline{O}_0$ to $\overline{O}_3$	complementary parallel latch outputs

TRUTH TABLE

E_0	E_1	latch condition
L	L	enabled
L	H	not enabled
H	L	not enabled
H	H	enabled



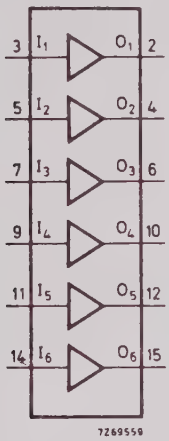


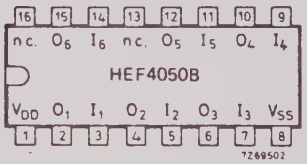
GENERAL DESCRIPTION

The HEF4042P is a 4-bit latch with four data inputs (D_0 to D_3), four buffered latch outputs (O_0 to O_3), four buffered complementary latch outputs ($\overline{O}_0$ to $\overline{O}_3$) and two common enable inputs (E_0 and E_1).
Information on D_0 to D_3 is transferred to O_0 to O_3 while both E_0 and E_1 are in the same state, either HIGH or LOW. O_0 to O_3 follow D_0 to D_3 as long as both E_0 and E_1 remain in the same state. When E_0 and E_1 are different, D_0 to D_3 do not affect O_0 to O_3 and the information in the latch is stored.
$\overline{O}_0$ to $\overline{O}_3$ are always the complement of O_0 to O_3. The exclusive-OR input structure allows the choice of either polarity for E_0 and E_1. With one enable input HIGH, the other enable input is active HIGH; with one enable input LOW, the other enable input is active LOW.

HEX NON–INVERTING BUFFERS — HEF4050B

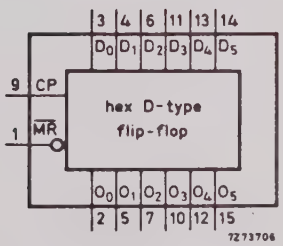
The HEF4050B provides six non-inverting buffers with high current output capability suitable for driving TTL or high capacitive loads. Since input voltages in excess of the buffers' supply voltage are permitted, the buffers may also be used to convert logic levels of up to 15 V to standard TTL levels. Their guaranteed fan-out into common bipolar logic elements is shown in the table on page 2.

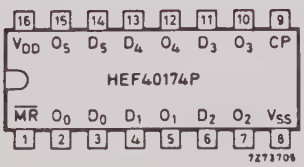




HEF4050BP: 16-lead DIL; plastic (SOT-38Z).
HEF4050BD: 16-lead DIL; ceramic (SOT-74).

HEX D-TYPE FLIP-FLOP — HEF40174P





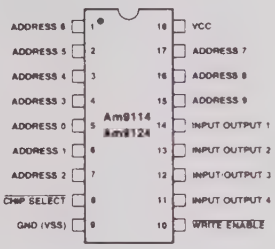
GENERAL DESCRIPTION

The HEF40174P is a hex edge-triggered D-type flip-flop with six data inputs (D_0 to D_5), a clock input (CP) an overriding asynchronous master reset input ($\overline{MR}$), and six buffered outputs (O_0 to O_5).
Information on D_0 to D_5 is transferred to O_0 to O_5 on the LOW-to-HIGH transition of CP if $\overline{MR}$ is HIGH. When LOW, $\overline{MR}$ resets all flip-flops (O_0 to O_5 = LOW) independent of CP and D_0 to D_5.

DISTINCTIVE CHARACTERISTICS

- **LOW OPERATING POWER (MAX)**
  Am9124/Am9114 368mW (70mA)
  Am91L24/Am91L14 262mW (50mA)
- **LOW STANDBY POWER (MAX)**
  Am9124 158mW (30mA)
  Am91L24 105mW (20mA)
- Access times down to 200ns (max)
- Military temperature range available to 300ns (max)
- Am9114 is a direct plug-in replacement for 2114
- Am9124 pin and function compatible with Am9114 and 2114, plus $\overline{CS}$ power down feature
- Fully static – no clocking
- Identical access and cycle time
- High output drive –
  4.0mA sink current @ 0.4V – 9124
  3.2mA sink current @ 0.4V – 9114
- TTL identical input/output levels
- 100% MIL-STD-883 reliability assurance testing

CONNECTION DIAGRAM



Top View
Pin 1 is marked for orientation.

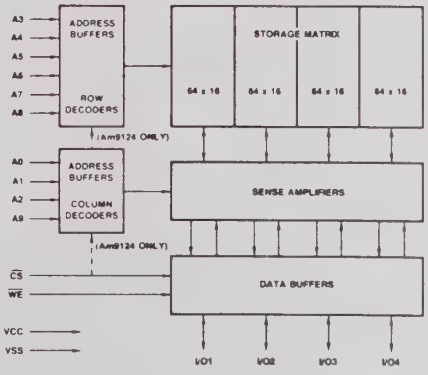
GENERAL DESCRIPTION

The Am9114 and Am9124 are high performance, static, N-Channel, read/write, random access memories organized as 1024 x 4. Operation is from a single 5V supply, and all input/output levels are identical to standard TTL specifications. Low power versions of both devices are available with power savings of over 30%. The Am9114 and Am9124 are the same except that the Am9124 offers an automatic $\overline{CS}$ power down feature.

The Am9124 remains in a low power standby mode as long as $\overline{CS}$ remains high, thus reducing its power requirements. The Am9124 power decreases from 368mW to 158mW in the standby mode, and the Am91L24 from 262mW to 105mW. The $\overline{CS}$ input does not affect the power dissipation of the Am9114. (See Figure 1, page 4).

Data readout is not destructive and the same polarity as data input. $\overline{CS}$ provides for easy selection of an individual package when the outputs are OR-tied. The outputs of 4.0mA for Am9124 and 3.2mA for Am9114 provides increased short circuit current for improved capacitive drive.

BLOCK DIAGRAM



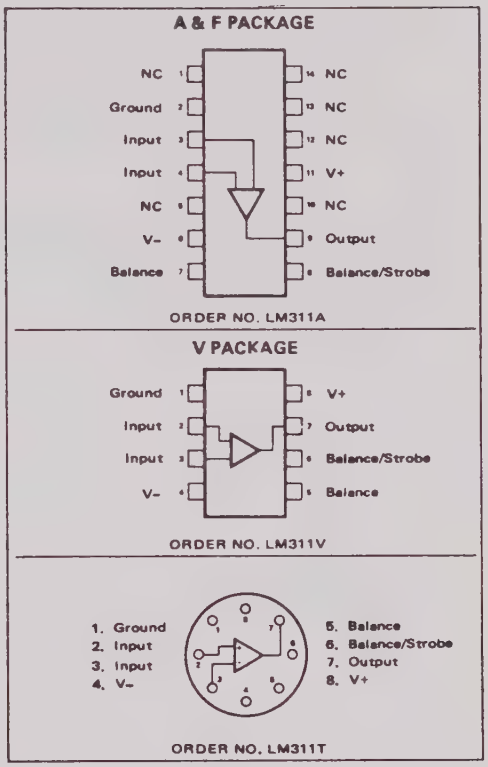
DESCRIPTION

The LM111 series are voltage comparators that have input currents approximately a hundred times lower than devices like the μA710. They are designed to operate over a wider range of supply voltages; from standard ±15V op amp supplies down to the single 5V supply used for IC logic. Their output is compatible with RTL, DTL, and TTL as well as MOS circuits. Further, they can drive lamps or relays, switching voltages up to 50V at currents as high as 50mA.

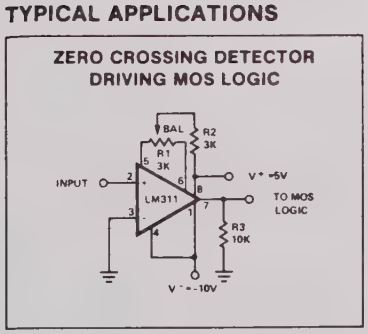
Both the inputs and the outputs of the LM111 series can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'ed. Although slower than the μA710 (200ns response time vs 40ns) the devices are also much less prone to spurious oscillations. The LM111 series has the same pin configuration as the μA710 series.

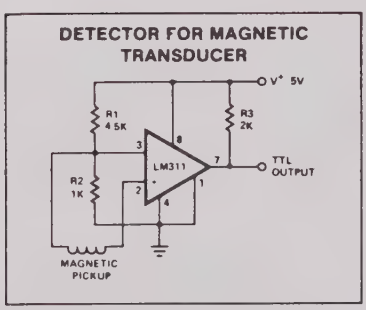
The LH2111 series hybrids are 2 LM111 type comparators in one hermetic package. They feature the same electrical parameters as the single devices.

PIN CONFIGURATION (Top View)

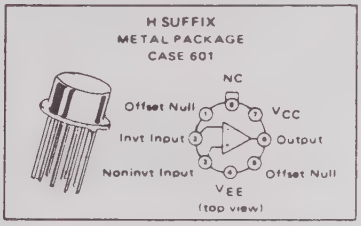


TYPICAL APPLICATIONS





HIGH PERFORMANCE JFET OP AMPS — LF 355 LF 356 LF 357 SERIES

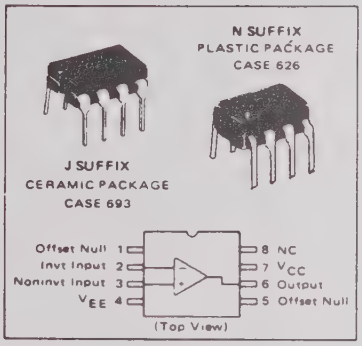


MONOLITHIC JFET INPUT OPERATIONAL AMPLIFIERS

These internally compensated operational amplifiers incorporate highly matched JFET devices on the same chip with standard bipolar transistors. The JFET devices enhance the input characteristics of these operational amplifiers by more than an order of magnitude over conventional amplifiers.

This series of op amps combines the low current characteristics typical of FET amplifiers with the low initial offset voltage and offset voltage stability of bipolar amplifiers. Also, nulling the offset voltage does not degrade the drift or common mode rejection.

- Low Input Bias Current – 30 pA
- Low Input Offset Current – 3.0 pA
- Low Input Offset Voltage – 1.0 mV
- Temperature Compensation of Input Offset Voltage – 3.0 $\mu V/^{o}C$
- Low Input Noise Current – 0.01 $pA/\sqrt{Hz}$
- High Input Impedance – $10^{12}\Omega$
- High Common-Mode Rejection Ratio – 100 dB
- High DC Voltage Gain – 106 dB



APPLICATIONS

The LF series is suggested for all general purpose FET input amplifier requirements where precision and frequency response flexibility are of prime importance.

Specific applications include:

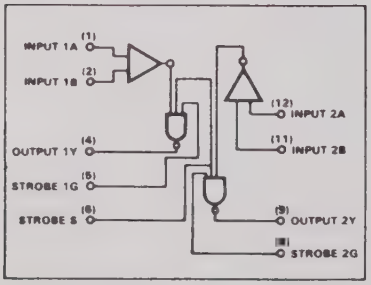
- Sample and Hold Circuits
- High Impedance Buffers
- Fast D/A and A/D Converters
- Precision High-Speed Integrators
- Wideband, Low Noise, Low Drift Amplifiers

HIGH SPEED DUAL DIFFERENTIAL COMPARATOR/SENSE AMP — NE/SE522

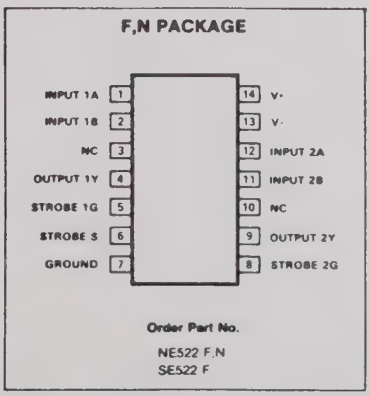
FEATURES

- **15ns maximum guaranteed propagation delay**
- **20μA maximum input bias current**
- **TTL compatible strobes and outputs**
- **Open collector output for wire-OR'd applications**
- **Large common mode input voltage range**
- **Operates from standard supply voltages**

BLOCK DIAGRAM



PIN CONFIGURATION



DESCRIPTION

The 5007/5008 series of 8-bit monolithic multiplying Digital-to-Analog Converters provide very high speed performance coupled with low cost and outstanding applications flexibility.

Advanced circuit design achieves 85ns settling times with very low glitch and at low power consumption. Monotonic multiplying performance is attained over a wide 40 to 1 reference current range. Matching to within 1 LSB between reference and full scale currents eliminates the need for full scale trimming in most applications. Direct interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic inputs.

Dual complementary outputs are provided, increasing versatility and enabling differential operation to effectively double the peak-to-peak output swing. True high voltage compliance outputs allow direct output voltage conversion and eliminate output op amps in many applications.

All 5007/5008 series models guarantee full 8-bit monotonicity and linearities as tight as 0.1% over the entire operating temperature range are available. Device performance is essentially unchanged over the ±4.5V to ±18V power supply range, with 33mW power consumption attainable at ±5V supplies.

The compact size and low power consumption make the 5007/5008 attractive for portable and military/aerospace applications.

FEATURES

- **Fast settling output current—85ns**
- **Full scale current prematched to ±1 LSB**
- **Direct interface to TTL, CMOS, ECL, HTL, PMOS**
- **Relative accuracy to 0.1% maximum over temperature range**
- **High output compliance—-10V to +18V**
- **True and complemented outputs**
- **Wide range multiplying capability**
- **Low FS current drift—±10ppm/°C**
- **Wide power supply range—±4.5V to ±18V**
- **Low power consumption—33mW at ±5V**
- **SE5008 military qualifications pending**

APPLICATIONS

- **8-bit, 1μs A-to-D converters**
- **Servo-motor and pen drivers**
- **Waveform generators**
- **Audio encoders and attenuators**
- **Analog meter drivers**
- **Programmable power supplies**
- **CRT display drivers**
- **High speed modems**
- **Other applications where low cost, high speed and complete input/output versatility are required**

ORDERING INFORMATION

RELATIVE ACCURACY	0 to 70°C	-55 to 125°C
0.39% FS	NE5007N NE5007F	
0.19% FS	NE5008N NE5008F	SE5008F

DEFINITION OF TERMS

Accuracy—The maximum deviation of the Dac output relative to an ideal straight line drawn from zero to full scale; 1 LSB for any bit combination

Differential linearity—The incremental error from an ideal 1 LSB analog output change when the digital input is changed 1 LSB; guaranteed monotonicity requires the differential linearity error be less than 1 LSB and with a tempco of essentially zero

Full scale tempco—The change in Dac full scale current with change in temperature expressed in ppm/°C

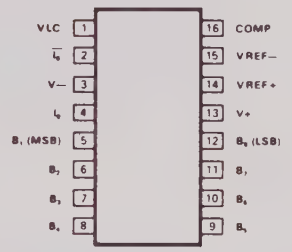
Monotonicity—For a 1 LSB increase of input code, the output either increases or remains the same

Output voltage compliance—The range of allowable voltage levels the output pins can assume without a major effect on circuit performance

Power supply sensitivity—The change in Dac output current with changes in power supply voltage

PIN CONFIGURATION

F,N PACKAGE*



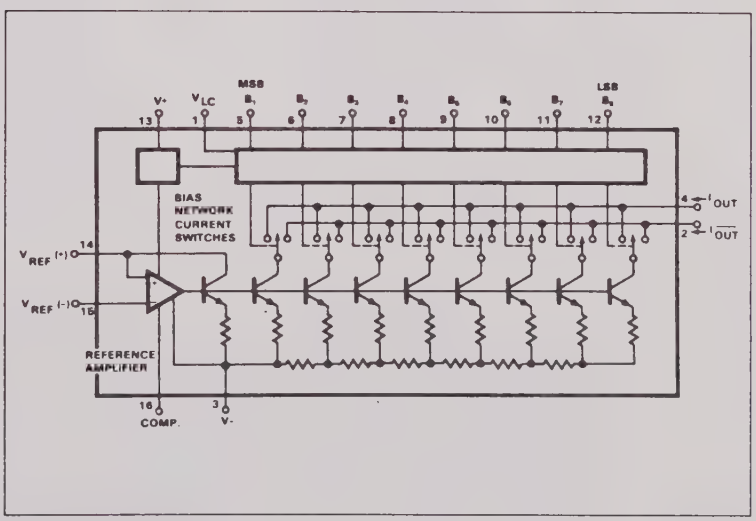
*N = Plastic DIP
F = Cerdip

CROSS REFERENCE

The 5007/5008 series are pin and functionally compatible with the DAC-08 series of devices.

PMI	SIGNETICS
DAC-08A	SE5009
DAC-08	SE5008
DAC-08H	NE5009
DAC-08E	NE5008
DAC-08C	NE5007

BLOCK DIAGRAM



- **Fast Access Time**
  - **— 350 ns Max. 2716-1**
  - **— 390 ns Max. 2716-2**
  - **— 450 ns Max. 2716**
- **Single +5V Power Supply**
- **Low Power Dissipation**
  - **— 525 mW Max. Active Power**
  - **— 132 mW Max. Standby Power**
- **Pin Compatible to Intel® 5V ROMs (2316E, 2332, and 2364) and 2732 EPROM**
- **Simple Programming Requirements**
  Single Location Programming
  Programs with One 50 ms Pulse
- **Inputs and Outputs TTL Compatible during Read and Program**
- **Completely Static**

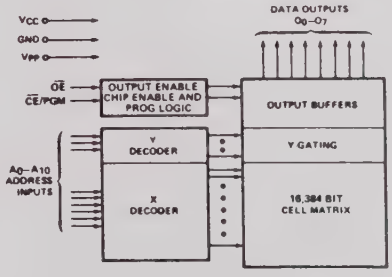
The Intel® 2716 is a 16,384-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 2716 operates from a single 5-volt power supply, has a static standby mode, and features fast single address location programming. It makes designing with EPROMs faster, easier and more economical. For production quantities, the 2716 user can convert rapidly to Intel's pin-for-pin compatible 16K ROM (the 2316E) or the new 32K and 64K ROMs (the 2332 and 2364 respectively).

The 2716, with its single 5-volt supply and with an access time up to 350 ns, is ideal for use with the newer high performance +5V microprocessors such as Intel's 8085 and 8086. The 2716 is also the first EPROM with a static standby mode which reduces the power dissipation without increasing access time. The maximum active power dissipation is 525 mW while the maximum standby power dissipation is only 132 mW, a 75% savings.

The 2716 has the simplest and fastest method yet devised for programming EPROMs — single pulse TTL level programming. No need for high voltage pulsing because all programming controls are handled by TTL signals. Now, it is possible to program on-board, in the system, in the field. Program any location at any time — either individually, sequentially or at random, with the 2716's single address location programming. Total programming time for all 16,384 bits is only 100 seconds.

PIN CONFIGURATION*

BLOCK DIAGRAM



MODE SELECTION

MODE \ PINS	CE/PGM (18)	OE (20)	VPP (21)	VCC (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

PIN NAMES

A_0–A_8	ADDRESSES
CE/PGM	CHIP ENABLE/PROGRAM
OE	OUTPUT ENABLE
O_0–O_7	OUTPUTS

32K (4K x 8) UV ERASABLE PROM — 2732

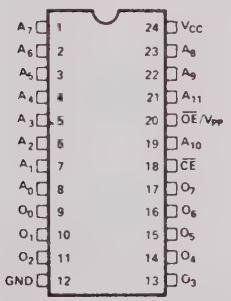
- **Single +5V ± 5% Power Supply**
- **Output Enable for MCS-85™ and MCS-86™ Compatibility**
- **Fast Access Time: 450ns Max.**
- **Low Power Dissipation:**
  160mA Max. Active Current
  25mA Max. Standby Current
- **Pin Compatible to Intel® 2716 EPROM and 2332/2364 ROMs**
- **Completely Static**
- **Simple Programming Requirements**
  — Single Location Programming
  — Programs with One 50ms Pulse
- **Three-State Output for Direct Bus Interface**

The Intel® 2732 is a 32,768-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 2732 operates from a single 5-volt power supply, has a standby mode, and features an output enable control. For production, the pin compatible 2332 and 2364 ROMs are available. The total programming time for all bits is three and a half minutes. All these features make designing with the 2732 in microcomputer systems faster, easier, and more economical.

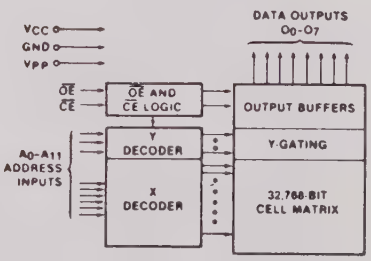
An important 2732 feature is the separate output control, Output Enable ($\overline{OE}$), from the Chip Enable control ($\overline{CE}$). The $\overline{OE}$ control eliminates bus contention in multiple bus microprocessor systems. Intel's Application Note AP-30 describes the microprocessor system implementation of the $\overline{OE}$ and $\overline{CE}$ controls on Intel's 2716 and 2732 EPROMs. AP-30 is available from Intel's Literature Department.

The 2732 has a standby mode which reduces the power dissipation without increasing access time. The maximum active current is 160mA, while the maximum standby current is only 25mA, an 85% savings. The standby mode is achieved by applying a TTL-high signal to the $\overline{CE}$ input.

PIN CONFIGURATION



BLOCK DIAGRAM



MODE SELECTION

MODE \ PINS	$\overline{CE}$ (18)	$\overline{OE}/V_{PP}$ (20)	V_{CC} (24)	OUTPUTS (9-11,13-17)
Read	V_{IL}	V_{IL}	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	High Z
Program	V_{IL}	V_{IHP}	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+5	D_{OUT}
Program Inhibit	V_{IH}	V_{IHP}	+5	High Z

PIN NAMES

A_0-A_{11}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	OUTPUTS

FUNCTIONAL PIN DEFINITION (as used in the PM 3543) — uP 8085

The following describes the function of the used pins.

$AD_{0\text{-}7}$ (input/output 3-state)

Multiplexed Address/Data Bus: Lower 8-bits of the memory address (or I/O address) appear on the bus during the first clock pulse. It then becomes the data bus during the second and third clock pulse of each machine cycle.

3-stated during Hold and Halt modes.

A_1-A_{15} (Output 3-State)

Address Bus: The most significant 8-bits of the memory address.

ALE (Output 3-state)

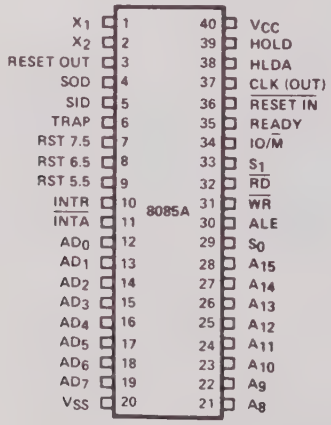
Address Latch Enable: It occurs during the first clock pulse of each machine cycle and enables the address to get latched into the address latch.
The falling edge of ALE is set to guarantee setup and hold times for the address information.

CLK (Output)

Clock Output for use when a crystal network is used as an input to CPU.

READY (Input)

If Ready is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If Ready is low, the CPU will wait for Ready to go high before completing the read or write cycle.



V_{CC}

+5 volt supply.

V_{SS}

Ground Reference.

X_1, X_2 (input)

Crystal network connections to set the clock generator.

RESET IN (input)

Reset sets the Program Counter to zero. The CPU is held in the reset condition as long as Reset is applied.

RESET OUT (Output)

Indicates CPU is being reset. Can be used as a system reset. The signal is synchronized to the processor clock and lasts an integral number of clock periods.

$\overline{RD}$ (Output 3-state)

READ: indicates the selected memory or I/O position is to be read and that the Data Bus is available for the data transfer.

$\overline{WR}$ (Output 3-state)

WRITE: indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of WR.

SID (input)

Serial input data line. The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.

SOD (Output)

Serial output data line. The output SOD is set or reset as specified by the SIM instruction.

HOLD (input)

HOLD indicates that another master is requesting the use of the address and data buses. The CPU, upon receiving the hold request, will relinquish the use of the bus as soon as the completion of the current bus transfer. Internal processing can continue.
The processor can regain the bus only after the HOLD is removed.
When the HOLD is acknowledged, the Address, Data, $\overline{RD}$, $\overline{WR}$, and IO/$\overline{M}$ lines are 3-stated.

RST 5.5, RST 6.5, RST 7.5 (Inputs)

RESTART INTERRUPTS: These three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted.

The priority of these interrupts is ordered as shown in Table 1. These interrupts have a higher priority than INTR. In addition, they may be individually masked out using the SIM instruction.

S_0, S_1, AND IO/$\overline{M}$ (Output)

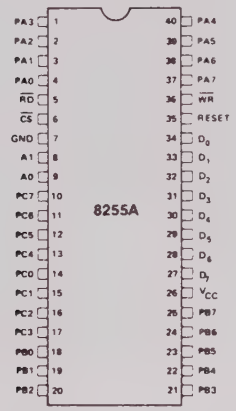
Machine cycle status:

IO/$\overline{M}$	S_1	S_0	Status
0	0	1	Memory write
0	1	0	Memory read
1	0	1	I/O write
1	1	0	I/O read
0	1	1	Opcode fetch
1	1	1	Interrupt Acknowledge

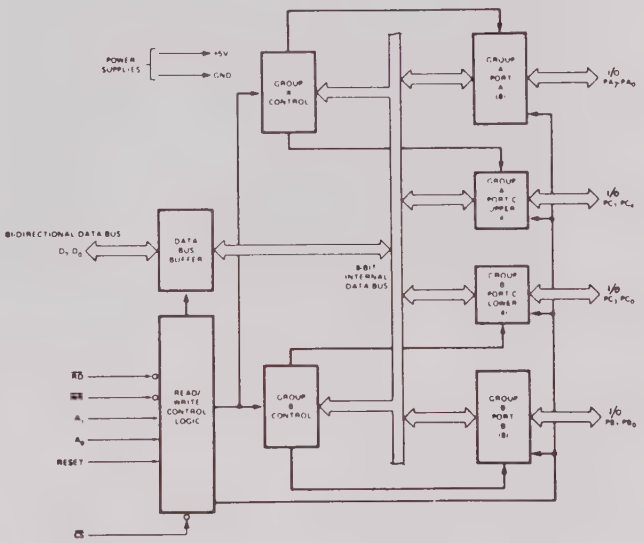
The 8255A is a general purpose programmable I/O device designed for use with both the 8008 and 8080 microprocessors. It has 24 I/O pins which may be individually programmed in two groups of twelve and used in three major modes of operation. In the first mode (Mode 0), each group of twelve I/O pins may be programmed in sets of 4 to be input or output. In Mode 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining four pins three are used for handshaking and interrupt control signals. The third mode of operation (Mode 2) is a Bi-directional Bus mode which uses 8 lines for a bi-directional bus, and five lines, borrowing one from the other group, for handshaking.

Other features of the 8255A include bit set and reset capability and the ability to source 1 mA of current at 1.5 volts. This allows darlington transistors to be directly driven for applications such as printers and high voltage displays.

PIN CONFIGURATION



8255A BLOCK DIAGRAM



PIN NAMES

D_7–D_0	DATA BUS (BI-DIRECTIONAL)
RESET	RESET INPUT
$\overline{CS}$	CHIP SELECT
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A0, A1	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7-PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
V_{CC}	+5 VOLTS
GND	0 VOLTS

8255 BASIC FUNCTIONAL DESCRIPTION

General

The 8255 is a Programmable Peripheral Interface (PPI) device designed for use in 8080 Microcomputer Systems. Its function is that of a general purpose I/O component to interface peripheral equipment to the 8080 system bus. The functional configuration of the 8255 is programmed by the system software so that normally no external logic is necessary to interface peripheral devices or structures.

Data Bus Buffer

This 3-state, bi-directional, eight bit buffer is used to interface the 8255 to the 8080 system data bus. Data is transmitted or received by the buffer upon execution of INput or OUTput instructions by the 8080 CPU. Control Words and Status information are also transferred through the Data Bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the 8080 CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

($\overline{CS}$)

Chip Select: A "low" on this input pin enables the communication between the 8255 and the 8080 CPU.

($\overline{RD}$)

Read: A "low" on this input pin enables the 8255 to send the Data or Status information to the 8080 CPU on the Data Bus. In essence, it allows the 8080 CPU to "read from" the 8255.

($\overline{WR}$)

Write: A "low" on this input pin enables the 8080 CPU to write Data or Control words into the 8255.

(A_0 and A_1)

Port Select 0 and Port Select 1: These input signals, in conjunction with the $\overline{RD}$ and $\overline{WR}$ inputs, control the selection of one of the three ports or the Control Word Register. They are normally connected to the least significant bits of the Address Bus (A_0 and A_1).

8255 BASIC OPERATION

A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	INPUT OPERATION (READ)
0	0	0	1	0	PORT A → DATA BUS
0	1	0	1	0	PORT B → DATA BUS
1	0	0	1	0	PORT C → DATA BUS
					OUTPUT OPERATION (WRITE)
0	0	1	0	0	DATA BUS → PORT A
0	1	1	0	0	DATA BUS → PORT B
1	0	1	0	0	DATA BUS → PORT C
1	1	1	0	0	DATA BUS → CONTROL
					DISABLE FUNCTION
X	X	X	X	1	DATA BUS → 3-STATE
1	1	0	1	0	ILLEGAL CONDITION
X	X	1	1	0	DATA BUS → 3-STATE

256 x 4-BIT FULLY DECODED RANDOM ACCESS MEMORY — 93422

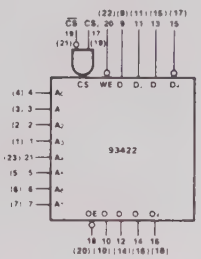
DESCRIPTION – The 93422 is a 1024-bit Read/Write Access Memory organized 256 words by four bits per word. The 93422 has 3-state outputs, and is designed primarily for buffer control storage and high-performance main memory applications. The device has a typical address access time of 30 ns.

- ISOPLANAR TECHNOLOGY
- ORGANIZATION – 256 WORDS X 4 BITS
- 3-STATE OUTPUTS
- STANDARD 22-PIN DUAL IN-LINE PACKAGE
- TWO CHIP SELECT INPUTS PROVIDE EASY MEMORY EXPANSION
- POWER DISSIPATION – 0.475 mW BIT TYPICAL
- TYPICAL READ ACCESS TIME – 30 ns

PIN NAMES

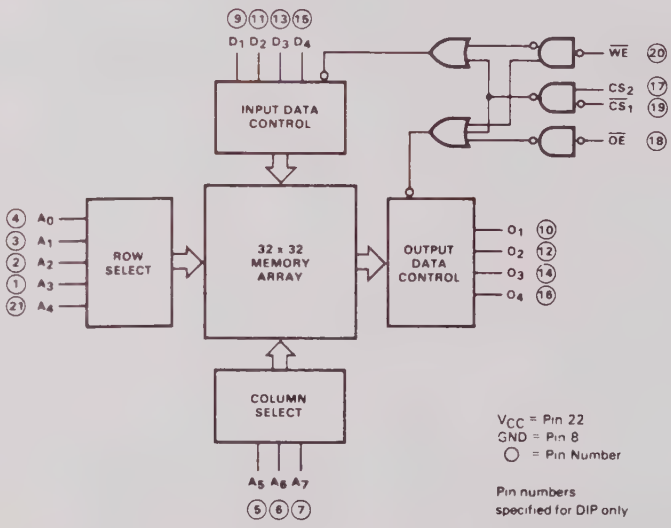
$A_0 - A_7$	Address Inputs
$D_1 - D_4$	Data Inputs
$\overline{CS}_1$, CS_2	Chip Select Inputs
$\overline{WE}$	Write Enable Input
$O_1 - O_4$	Data Outputs
$\overline{OE}$	Output Enable

LOGIC SYMBOL

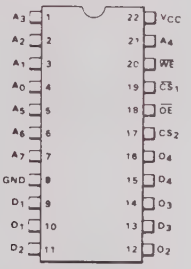


V_{CC} = Pin 22 (24)
GND = Pin 8
( ) = FLATPAK

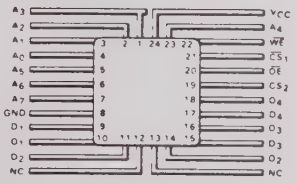
LOGIC DIAGRAM



CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



FUNCTIONAL DESCRIPTION — The 93422 is a fully decoded 1024-bit Random Access Memory organized 256 words by four bits. Word selection is achieved by means of an 8-bit address, A_0 through A_7.

Two Chip Select inputs are provided for logic flexibility. For larger memories, the fast chip select access time permits the decoding of Chip Select, CS, from the address without increasing address access time.

The read and write operations are controlled by the state of the active LOW Write Enable, $\overline{WE}$ (pin 20). With $\overline{WE}$ held LOW and the chip selected, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held HIGH and the chip selected. Data in the specified location is presented at D_{OUT} and is not inverted.

TRUTH TABLE

INPUTS					OUTPUTS	
$\overline{OE}$ PIN 18	$\overline{CS}_1$ PIN 19	CS_2 PIN 17	$\overline{WE}$ PIN 20	$D_1 - D_4$ PINS 9, 11,13, 15	3-STATE	MODE
X	H	X	X	X	HIGH Z	Not Selected
X	X	L	X	X	HIGH Z	Not Selected
L	L	H	H	X	$O_1 - O_4$	Read Stored Data
X	L	H	L	L	HIGH Z	Write "0"
X	L	H	L	H	HIGH Z	Write "1"
H	L	H	H	X	HIGH Z	Output Disabled
H	L	H	L	L	HIGH Z	Write "0" (Output Disabled)
H	L	H	L	H	HIGH Z	Write "1" (Output Disabled)

H = HIGH Voltage, L = LOW Voltage, X = Don't Care (HIGH or LOW), HIGH Z = High Impedance
NOTE Pin number specified for DIP only

7. PARTS LISTS AND DIAGRAMS (Subject to alterations without notice)

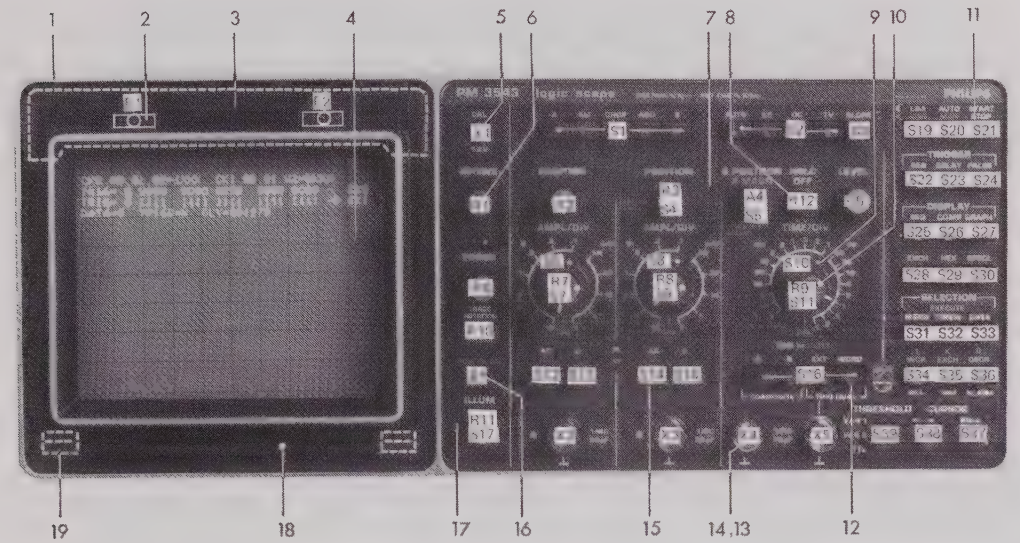


Fig.7.1. Front view showing item numbers

7.1.Mechanical parts

Item	Qty	Ordering number	Designation
1	1	5322 447 94401	Cast aluminium front frame
2	2	5322 225 24015	Lamp holder
3	2	5322 381 14151	Reflector
4	1	5322 480 34074	Contrast filter blue
5		5322 325 84013	Grommet for X1
6	8	5322 414 34134	Knob (dia 10)
6	7	5322 414 74015	Knob cover grey
6	8	5322 492 64337	Retaining spring
7	2	5322 414 34091	Knob (dia 10)
8	1	5322 414 34217	Knob (dia 10)
9	3	5322 414 34079	Knob (dia 18,7)
10	3	5322 414 74029	Knob cover blue
11	1	5322 414 26019	Knob square light-grey
12	30	5322 414 14011	Knob square grey
13	1	5322 505 14178	Knurled nut
14	1	5322 506 14005	Hexagonal nut
15	5	5322 414 25613	Knob square grey-green
16	1	5322 255 44088	LED holder
17	1	5322 455 81001	Text plate (PM 3542)
17		5322 455 84103	Text plate (PM 3543)
18	1	5322 450 74009	Bezel74009
19	2	5322 492 64629	Bezel clamp spring

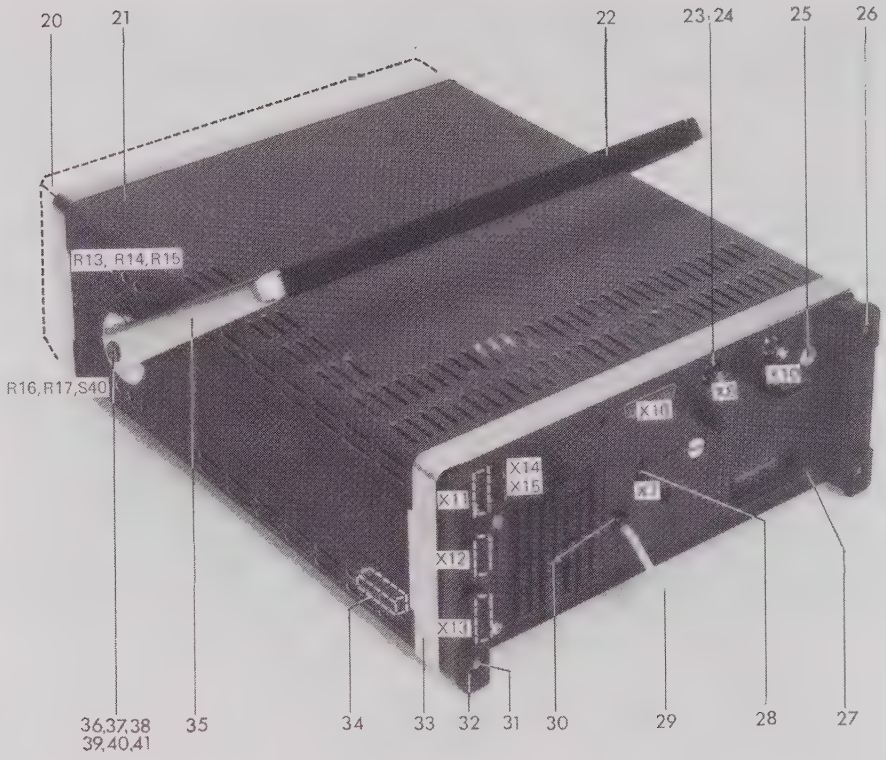


Fig.7.2. Side view showing item numbers

Item	Qty	Ordering number	Designation
20	1	5322 447 94403	Front cover
21	1	5322 447 94646	Cabinet without handle
22	1	5322 498 54077	Grip
23	2	5322 506 14001	Nut for X8 and X10
24	2	5322 532 24319	Padding ring for X8 and X10
25	2	5322 500 14228	Coin slot screw
26	1	5322 462 44298	Foot
27	1	5322 447 90017	Rear panel
28	1	5322 272 10215	Line voltage adaptor
29	1	4822 321 10084	Line cable (Eur.)
29	1	4822 321 10092	Line cable (U.S.A.)
30	1	5322 325 64083	Line cable cleat
31	4	5322 462 44374	Hole plug
32	1	5322 462 44474	Foot
33	1	5322 447 94647	Cast aluminium rear frame
34	4	5322 462 44297	Foot
35	2	5322 498 54072	Carrying handle
36	2	5322 414 64053	Knob
37	2	4822 50 30054	Screw
38	2	4822 532 10582	Washer
39	2	5322 528 34128	Ratched
40	2	5322 530 84075	Spring
41	2	5322 520 14267	Bearing bush

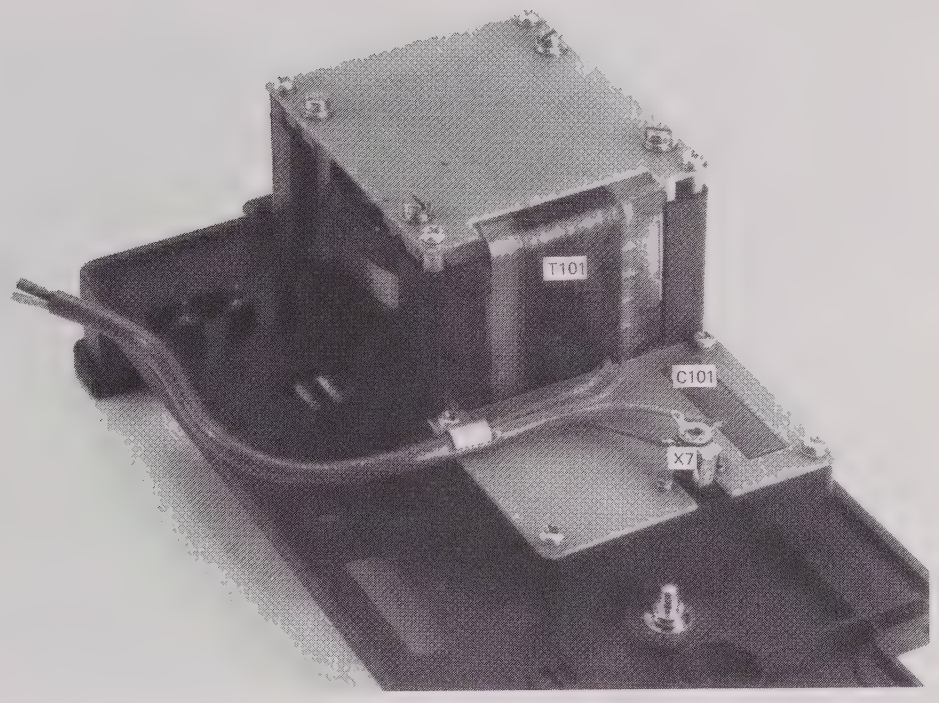


Fig.7.3. A.C.compartment showing item numbers

Note: For ordering numbers of T101, C101 and X7 see the relevant parts list.

Not shown in a figure are the following items :

Item	Ordering number	Designation
1	5322 532 74014	Rubber brace around socket of CRT.
2	5322 325 64051	Rubber cable grommet (2x)
3	5322 705 34066	Insulating plate for R6
4	4822 532 60711	Insulating Bush for R6
5	4822 255 40115	Insulating material for transist. V207
6	5322 276 14102	Self-releasing push-button segment
7	5322 276 14117	Mutual-releasing push-button segment
8	5322 255 44217	I.C. socket 40-pins
9	5322 255 44109	I.C. socket 24-pins
10	5322 532 64293	Contact bush for X16, X17 enz.

7.2. Electrical parts

ITEM	FARAD/TOL (%)	VOLTS	ORDERING NUMBER
CAPACITORS			
C 11	4,7PF 0,25PF	100	4822 122 31045
C 12	18PF 2	100	4822 122 31061
C 13	10NF-20+80	40	4822 122 30043
C 14	10NF-20+80	40	4822 122 30043
C 17	10NF-20+80	40	4822 122 30043
C 21	4,7PF 0,25PF	100	4822 122 31045
C 22	18PF 2	100	4822 122 31061
C 27	10NF-20+80	40	4822 122 30043
C 31	4,7PF 0,25PF	100	4822 122 31045
C 32	18PF 2	100	4822 122 31061
C 33	10NF-20+80	40	4822 122 30043
C 34	10NF-20+80	40	4822 122 30043
C 37	10NF-20+80	40	4822 122 30043
C 41	4,7PF 0,25PF	100	4822 122 31045
C 42	18PF 2	100	4822 122 31061
C 47	10NF-20+80	40	4822 122 30043
C 51	4,7PF 0,25PF	100	4822 122 31045
C 52	18PF 2	100	4822 122 31061
C 53	10NF-20+80	40	4822 122 30043
C 54	10NF-20+80	40	4822 122 30043
C 57	10NF-20+80	40	4822 122 30043
C 61	4,7PF 0,25PF	100	4822 122 31045
C 62	18PF 2	100	4822 122 31061
C 67	10NF-20+80	40	4822 122 30043
C 71	4,7PF 0,25PF	100	4822 122 31045
C 72	18PF 2	100	4822 122 31061
C 73	10NF-20+80	40	4822 122 30043
C 74	10NF-20+80	40	4822 122 30043
C 77	10NF-20+80	40	4822 122 30043
C 81	4,7PF 0,25PF	100	4822 122 31045
C 82	18PF 2	100	4822 122 31061
C 87	10NF-20+80	40	4822 122 30043
C 91	15UF-10+50	16	4822 124 20687
C 92	10NF-20+80	40	4822 122 30043
C 93	15UF-10+50	16	4822 124 20687
C 94	15UF-10+50	16	4822 124 20687
C 95	10NF-20+80	40	4822 122 30043
C 96	15UF-10+50	16	4822 124 20687
C 97	10NF-20+80	40	4822 122 30043
C 98	10NF-20+80	40	4822 122 30043
C 99	10NF-20+80	40	4822 122 30043
C 101	220NF—10	275	5322 121 54261
C 200	100NF 10%	250V	4822 121 41161
C 201	3,3NF 10	100	4822 122 30099
C 202	680NF 10%	100V	4822 121 40443
C 203	4700UF-10+50	40	4822 124 70226
C 204	100NF 10%	250V	4822 121 41161
C 207	100NF 10%	630V	4822 121 40145
C 208	47UF-10+50	25	4822 124 20699
C 209	10UF-10+50	25	4822 124 20697
C 211	68UF-10+50	6,3	4822 124 20671
C 212	470PF 20%	4KV	5322 122 54004
C 213	470PF 20%	4KV	5322 122 54004
C 214	470PF 20%	4KV	5322 122 54004
C 216	470PF 20%	4KV	5322 122 54004
C 217	470PF 20%	4KV	5322 122 54004
C 218	22NF 10%	1600V	4822 121 40196
C 219	22NF 10%	1600V	4822 121 40196
C 221	4,7UF-10+50	250	4822 124 21157
C 222	100UF-10+50	40	4822 124 20715
C 223	33UF-10+50	16	4822 124 20688
C 224	220UF-10+50	16	4822 124 20693

ITEM	FARAD/TOL (%)	VOLTS	ORDERING NUMBER
C 226	68UF-10+50	6,3	4822 124 20671
C 227	470UF-10+50	6,3	4822 124 20673
C 228	33UF-10+50	16	4822 124 20658
C 229	220UF-10+50	16	4822 124 20693
C 231	4,7UF-10+50	250	4822 124 21157
C 301	100NF 10%	400V	4822 121 40012
C 305	47PF 2	500	4822 122 31072
C 307	18PF		5322 125 50051
C 308	47PF 2	500	4822 122 31072
C 309	15PF 2	500	4822 122 31197
C 310	15PF 2	500	4822 122 31197
C 311	12PF 2	500	4822 122 31196
C 312	3,9PF 0,25PF	500	4822 122 31217
C 313	5,5PF	400	5322 125 54027
C 314	5,5PF	400	5322 125 54027
C 315	1,5PF 0,25PF	500	4822 122 31184
C 316	3PF	400	5322 125 54026
C 317	3PF	400	5322 125 54026
C 318	5,5PF	400	5322 125 54027
C 319	3PF	400	5322 125 54026
C 320	3,3PF 0,25PF	500	4822 122 31188
C 321	27PF 2	100	4822 122 30045
C 322	120PF 2	100	4822 122 31348
C 324	120PF 2	100	4822 122 31348
C 351	39PF 2	500	4822 122 31203
C 352	27PF 2	100	4822 122 30045
C 353	22NF-20+80	40	4822 122 30103
C 354	2,2PF 0,25PF	100	5322 122 34198
C 357	22NF-20+80	40	4822 122 30103
C 358	22NF-20+80	40	4822 122 30103
C 401	100NF 10%	400V	4822 121 40012
C 405	47PF 2	500	4822 122 31072
C 407	18PF		5322 125 50051
C 408	47PF 2	500	4822 122 31072
C 409	15PF 2	500	4822 122 31197
C 410	15PF 2	500	4822 122 31197
C 411	12PF 2	500	4822 122 31196
C 412	3,9PF 0,25PF	500	4822 122 31217
C 413	5,5PF	400	5322 125 54027
C 414	5,5PF	400	5322 125 54027
C 415	1,5PF 0,25PF	500	4822 122 31184
C 416	3PF	400	5322 125 54026
C 417	3PF	400	5322 125 54026
C 418	5,5PF	400	5322 125 54027
C 419	3PF	400	5322 125 54026
C 420	3,3PF 0,25PF	500	4822 122 31188
C 421	27PF 2	100	4822 122 30045
C 422	120PF 2	100	4822 122 31348
C 424	120PF 2	100	4822 122 31348
C 501	47PF 2	100	4822 122 31072
C 502	20PF	100	4822 125 50045
C 503	180PF 2	100	4822 122 31352
C 504	5,6PF 0,25PF	100	4822 122 31047
C 507	3,5PF	300	5322 125 50045
C 509	22NF-20+80	40	4822 122 30103
C 510	33PF 2	100	4822 122 31067
C 511	10PF 2	100	4822 122 31054
C 513	22NF-20+80	40	4822 122 30103
C 517	22NF-20+80	40	4822 122 30103
C 518	22NF-20+80	40	4822 122 30103
C 519	22NF-20+80	40	4822 122 30103
C 521	22NF-20+80	40	4822 122 30103
C 522	150PF 2	100	4822 122 31083
C 523	22NF-20+80	40	4822 122 30103
C 524	150F-10+50	16	4822 124 20687

ITEM	FARAD/TOL (%)	VOLTS	ORDERING NUMBER
C 527	15UF-10+50	16	4822 124 20687
C 528	22NF-20+80	40	4822 122 30103
C 529	15UF-10+50	16	4822 124 20687
C 530	22NF-20+80	40	4822 122 30103
C 531	15UF-10+50	16	4822 124 20687
C 532	22NF-20+80	40	4822 122 30103
C 601	47PF 2	100	4822 122 31072
C 602	20PF	100	4822 125 50045
C 603	180PF 2	100	4822 122 31352
C 604	5,6PF 0,25PF	100	4822 122 31047
C 607	3,5PF		5322 125 50048
C 609	22NF-20+80	40	4822 122 30103
C 610	33PF 2	100	4822 122 31067
C 611	10PF 2	100	4822 122 31054
C 613	22NF-20+80	40	4822 122 30103
C 616	22NF-20+80	40	4822 122 30103
C 617	22NF-20+80	40	4822 122 30103
C 618	22NF-20+80	40	4822 122 30103
C 619	22NF-20+80	40	4822 122 30103
C 621	22NF-20+80	40	4822 122 30103
C 622	150PF 2	100	4822 122 31085
C 623	22NF-20+80	40	4822 122 30103
C 627	15UF-10+50	16	4822 124 20687
C 629	15UF-10+50	16	4822 124 20687
C 630	22NF-20+80	40	4822 122 30103
C 631	15UF-10+50	16	4822 124 20687
C 632	22NF-20+80	40	4822 122 30103
C 701	22NF-20+80	40	4822 122 30103
C 702	270PF 10	100	4822 122 30095
C 703	2,7NF 10	100	4822 122 30057
C 704	2,7NF 10	100	4822 122 30057
C 705	4,7NF-20+80	40	4822 122 31125
C 706	22NF-20+80	40	4822 122 30103
C 707	22NF-20+80	40	4822 122 30103
C 709	100PF 2	500	4822 122 31081
C 801	22NF-20+80	40	4822 122 30103
C 802	18PF 2	100	4822 122 31061
C 803	3,3NF 10	100	4822 122 30099
C 804	180PF 2	100	4822 122 31352
C 805	1PF 0,25PF	100	4822 122 30104
C 806	1NF 10	100	4822 122 30027
C 807	56PF 2	100	4822 122 31074
C 808	47PF 2	100	4822 122 31072
C 809	40PF	250	4822 125 50092
C 810	1PF 0,25PF	100	4822 122 30104
C 811	40PF		4822 125 50092
C 812	33PF 2	100	4822 122 31067
C 813	22NF-20+80	40	4822 122 30103
C 814	10PF 2	100	4822 122 31054
C 815	22NF-20+80	40	4822 122 30103
C 816	10PF 2	100	4822 122 31054
C 818	3,5PF	300	5322 125 50048
C 821	22NF-20+80	40	4822 122 30103
C 827	33PF 2	100	4822 122 31067
C 1001	470NF 10%	100V	4822 121 40438
C 1002	470NF 10%	100V	4822 121 40438
C 1003	220NF 10%	100V	4822 121 40427
C 1004	22NF-20+80	40	4822 122 30103
C 1006	15UF-10+50	16	4822 124 20687
C 1007	22NF-20+80	40	4822 122 30103
C 1008	0,56PF 0,25PF	100	5322 122 34039
C 1011	4,7NF 10	100	4822 122 30128
C 1012	4,7NF 10	100	4822 122 30128
C 1013	3,9NF 10	100	4822 122 30098
C 1016	15UF-10+50	16	4822 124 20687

ITEM	FARAD/TOL (%)	VOLTS	ORDERING NUMBER
C 1017	22NF-20+80	40	4822 122 30103
C 1018	15UF-10+50	16	4822 124 20687
C 1019	15UF-10+50	16	4822 124 20687
C 1201	150PF 2	100	4822 122 31085
C 1202	150NF 10%	100V	4822 121 40423
C 1203	270PF 10	100	4822 122 30095
C 1204	2.4NF 1%	63V	5322 121 54054
C 1205	82PF 2	100	4822 122 31243
C 1206	10NF-20+50	100	4822 122 31414
C 1207	2.2UF 5%	100V	5322 121 44246
C 1208	4,7UF-10+50	63	4822 124 20726
C 1209	1NF 10	100	4822 122 30027
C 1210	22NF-20+80	40	4822 122 30103
C 1211	22NF-20+80	40	4822 122 30103
C 1212	22NF-20+80	40	4822 122 30103
C 1213	15UF-10+50	16	4822 124 20687
C 1214	15UF-10+50	16	4822 124 20687
C 1216	15UF-10+50	16	4822 124 20687
C 1220	22PF 2	100	4822 122 31063
C 1221	470PF 10	100	4822 122 30034
C 1401	22NF-20+80	40	4822 122 30103
C 1402	1NF 10	100	4822 122 30027
C 1404	220NF 10%	100V	4822 121 40427
C 1406	0,56PF 0,25PF	100	5322 122 34039
C 1407	0,56PF 0,25PF	100	5322 122 34039
C 1408	0,56PF 0,25PF	100	5322 122 34039
C 1409	3,5PF	300	5322 125 50048
C 1411	22NF-20+80	40	4822 122 30103
C 1412	22NF-20+80	40	4822 122 30103
C 1413	22NF 10%	250V	4822 121 40407
C 1414	22NF-20+80	40	4822 122 30103
C 1416	22NF 10%	250V	4822 121 40407
C 1417	100NF 10%	250V	4822 121 41161
C 1418	100NF 10%	250V	4822 121 41161
C 1419	100NF 10%	250V	4822 121 41161
C 1421	100NF 10%	250V	4822 121 41161
C 1501	22NF-20+80	40	4822 122 30103
C 1502	22NF-20+80	40	4822 122 30103
C 1503	22NF-20+80	40	4822 122 30103
C 1504	1PF 0,25PF	100	4822 122 30104
C 1506	10NF-20+80	40	4822 122 30043
C 1507	10NF	630V	4822 121 41134
C 1508	3,3NF 10	100	4822 122 30099
C 1509	1,5NF 10%	1600V	4822 121 40354
C 1511	22NF-20+80	40	4822 122 30103
C 1512	1,5NF 10%	1600V	4822 121 40354
C 1513	1,5NF 10%	1600V	4822 121 40354
C 1601	330NF 10%	100V	4822 121 40434
C 1602	47PF 2	100	4822 122 31072
C 2001	1000UF-10+50	10	5322 124 24249
C 2002	100UF-10+50	10	5322 124 24268
C 2101	33PF 2	100	4822 122 31067
C 2102	100NF-20+80	25	5322 122 34095
C 2103	10NF-20+80	40	4822 122 30043
C 2104	100NF-20+80	25	5322 122 34095
C 2106	100NF-20+80	25	5322 122 34095
C 2107	10NF-20+80	40	4822 122 30043
C 2108	100NF-20+80	25	5322 122 34095
C 2109	100NF-20+80	25	5322 122 34095
C 2111	100NF-20+80	25	5322 122 34095
C 2112	10NF-20+80	40	4822 122 30043
C 2113	10NF-20+80	40	4822 122 30043
C 2114	100NF-20+80	25	5322 122 34095
C 2116	100NF-20+80	25	5322 122 34095
C 2117	15PF 2	100	4822 122 31058

ITEM	FARAD/TOL (%)	VOLTS	ORDERING NUMBER
C 2118	56PF 2	100	4822 122 31074
C 2119	100NF-20+80	25	5322 122 34095
C 2120	18PF 2	100	4822 122 31061
C 2121	100NF-20+80	25	5322 122 34095
C 2122	100NF-20+80	25	5322 122 34095
C 2123	18PF 2	100	4822 122 31061
C 2124	100NF-20+80	25	5322 122 34095
C 2126	100NF-20+80	25	5322 122 34095
C 2127	100PF 2	100	4822 122 31316
C 2128	10NF-20+80	40	4822 122 30043
C 2129	100NF-20+80	25	5322 122 34095
C 2131	68PF 2	100	4822 122 31293
C 2132	100NF-20+80	25	5322 122 34095
C 2133	100PF 2	100	4822 122 31316
C 2134	100NF-20+80	25	5322 122 34095
C 2136	100NF-20+80	25	5322 122 34095
C 2137	33PF 2	100	5322 122 34145
C 2138	100NF-20+80	25	5322 122 34095
C 2139	15UF 50%	20V	5322 124 14036
C 2141	100NF-20+80	25	5322 122 34095
C 2142	6,8UF 20%	25V	5322 124 14081
C 2143	10NF-20+80	40	4822 122 30043
C 2144	10NF–20+80%	40V	4822 122 30043
C 2146	6,8UF 20%	25V	5322 124 14081
C 2201	68UF–10+50%	16V	4822 124 20689
C 2202	100NF–20+80%	25V	5322 122 34095
C 2203	100NF–20+80%	25V	5322 122 34095
C 2204	100NF–20+80%	25V	5322 122 34095
C 2205	100NF–20+80%	25V	5322 122 34095
C 2206	100NF–20+80%	25V	5322 122 34095
C 2207	100NF–20+80%	25	5322 122 34095
C 2300	100NF-20+80	25	5322 122 34095
C 2301	100NF-20+80	25	5322 122 34095
C 2302	100NF-20+80	25	5322 122 34095
C 2303	100NF-20+80	25	5322 122 34095
C 2304	100NF-20+80	25	5322 122 34095
C 2306	100NF-20+80	25	5322 122 34095
C 2307	100PF	200	5322 125 50046
C 2308	100PF	200	5322 125 50046
C 2309	100NF-20+80	25	5322 122 34095
C 2311	100NF-20+80	25	5322 122 34095
C 2312	100NF-20+80	25	5322 122 34095
C 2313	100NF-20+80	25	5322 122 34095
C 2314	100NF-20+80	25	5322 122 34095
C 2316	18PF 2	100	4822 122 31061
C 2317	100NF-20+80	25	5322 122 34095
C 2321	39PF 2	100	4822 122 31069
C 2322	39PF 2	100	4822 122 31069
C 2323	39PF 2	100	4822 122 31069
C 2324	39PF 2	100	4822 122 31069
C 2326	39PF 2	100	4822 122 31069
C 2327	100PF	200	5322 125 50046
C 2328	100PF	200	5322 125 50046
C 2329	100PF	200	5322 125 50046
C 2331	100PF	200	5322 125 50046
C 2332	100PF	200	5322 125 50046
C 2333	100PF	200	5322 125 50046
C 2334	100NF-20+80	25	5322 122 34095
C 2336	100NF-20+80	25	5322 122 34095
C 2337	100NF-20+80	25	5322 122 34095
C 2338	100NF-20+80	25	5322 122 34095
C 2339	100NF-20+80	25	5322 122 34095
C 2341	100NF-20+80	25	5322 122 34095

ITEM	FARAD/TOL (%)	VOLTS	ORDERING NUMBER
C 2342	100NF-20+80	25	5322 122 34095
C 2343	100NF-20+80	25	5322 122 34095
C 2344	100NF-20+80	25	5322 122 34095
C 2345	100NF-20+80	25	5322 122 34095
C 2346	100NF-20+80	25	5322 122 34095
C 2347	100NF-20+80	25	5322 122 34095
C 2348	100NF-20+80	25	5322 122 34095
C 2349	100NF-20+80	25	5322 122 34095
C 2354	100NF-20+80	25	5322 122 34095
C 2356	100NF-20+80	25	5322 122 34095
C 2357	100NF-20+80	25	5322 122 34095
C 2358	100NF-20+80	25	5322 122 34095
C 2359	100NF-20+80	25	5322 122 34095
C 2361	100NF-20+80	25	5322 122 34095
C 2362	100NF-20+80	25	5322 122 34095
C 2363	100NF-20+80	25	5322 122 34095
C 2364	100NF-20+80	25	5322 122 34095
C 2366	100NF-20+80	25	5322 122 34095
C 2367	100NF-20+80	25	5322 122 34095
C 2368	39PF 2	100	4822 122 31069
C 2369	39PF 2	100	4822 122 31069
C 2371	39PF 2	100	4822 122 31069
C 2372	39PF 2	100	4822 122 31069
C 2373	39PF 2	100	4822 122 31069
C 2374	39PF 2	100	4822 122 31069
C 2376	39PF 2	100	4822 122 31069
C 2377	39PF 2	100	4822 122 31069
C 2378	100PF	200	5322 125 50046
C 2379	100PF	200	5322 125 50046
C 2381	100PF	200	5322 125 50046
C 2382	100PF	200	5322 125 50046
C 2383	100PF	200	5322 125 50046
C 2384	100PF	200	5322 125 50046
C 2385	100NF-20+80	25	5322 122 34095
C 2387	100NF-20+80	25	5322 122 34095
C 2388	100NF-20+80	25	5322 122 34095
C 2389	100NF-20+80	25	5322 122 34095
C 2391	100NF-20+80	25	5322 122 34095
C 2392	100NF-20+80	25	5322 122 34095
C 2393	68UF-10+50	16	4822 124 20689
C 2394	100UF-10+50	10	4822 124 20679
C 2396	68UF-10+50	16	4822 124 20689
C 2397	100NF-20+80	25	5322 122 34095
C 2398	100NF-20+80	25	5322 122 34095
C 2399	47UF-10+50	63	4822 124 20733
C 2401	100NF-20+80	25	5322 122 34095
C 2402	22NF-20+80	40	4822 122 30103
C 2403	100NF-20+80	25	5322 122 34095
C 2404	100UF-10+50	10	4822 124 20679
C 2406	100NF-20+80	25	5322 122 34095
C 2407	39PF 2	100	4822 122 31069
C 2408	39PF 2	100	4822 122 31069
C 2409	39PF 2	100	4822 122 31069
C 2411	39PF 2	100	4822 122 31069
C 2412	39PF 2	100	4822 122 31069
C 2413	39PF 2	100	4822 122 31069
C 2414	39PF 2	100	4822 122 31069
C 2416	39PF 2	100	4822 122 31069

ITEM	FARAD/TOL (%)	VOLTS	ORDERING NUMBER
C 2417	100NF–20+80	25	5322 122 34095
C 2419	100PF	200	5322 125 50046
C 2421	100PF	200	5322 125 50046
C 2422	100PF	200	5322 125 50046
C 2423	100PF	200	5322 125 50046
C 2424	100PF	200	5322 125 50046
C 2426	100PF	200	5322 125 50046
C 2427	100PF	200	5322 125 50046
C 2428	100PF	200	5322 125 50046
C 2429	100PF	200	5322 125 50046
C 2431	100NF–20+80	25	5322 122 34095
C 2432	100NF–20+80	25	5322 122 34095
C 2433	100NF–20+80	25	5322 122 34095
C 2434	100NF–20+80	25	5322 122 34095
C 2442	10NF–20+80	40	4822 122 30043
C 2444	10NF–20+80	40	4822 122 30043

ITEM	OHM	TOL (%)	TYPE	ORDERING NUMBER
RESISTORS				
R 1	10K	20	0.1W	5322 101 24117
R 2	1K	20	0.1W	5322 101 24118
R 3	1K	20	0.1W	5322 101 64018
R 4	47K +47K	LIN	0,1W	5322 102 44004
R 5	100K	20	0.1W	4822 101 20457
R 6	2,2M	20	0.1W	5322 101 24098
R 7	1K	20	0.1W	5322 101 44024
R 8	1K	20	0.1W	5322 101 44024
R 9	10K	20	0.1W	5322 101 44023
R 11	22K	20	0.1W	5322 101 44025
R 12	47K	20	0.1W	5322 101 24197
R 13	100K	20	0,1W	5322 101 24178
R 14	47K	20	0.75W	5322 101 14056
R 15	10K	20	0.75W	5322 101 14217
R 16	10K	20	0.75W	5322 101 14217
R 17	10K	20	0.75W	5322 101 14217
R 21	4M	1	SPEC	5322 116 64025
R 22	681K	1	MR25	5322 116 55284
R 26	30,1	1	MR25	5322 116 50904
R 27	154K	1	MR25	5322 116 54714
R 31	4M	1	SPEC	5322 116 64025
R 32	681K	1	MR25	5322 116 55284
R 36	30,1	1	MR25	5322 116 50904
R 37	154K	1	MR25	5322 116 54714
R 41	4M	1	SPEC	5322 116 64025
R 42	681K	1	MR25	5322 116 55284
R 46	30,1	1	MR25	5322 116 50904
R 47	154K	1	MR25	5322 116 54714
R 51	4M	1	SPEC	5322 116 64025
R 52	681K	1	MR25	5322 116 55284
R 56	30,1	1	MR25	5322 116 50904
R 57	154K	1	MR25	5322 116 54714
R 61	4M	1	SPEC	5322 116 64025
R 62	681K	1	MR25	5322 116 55284
R 66	30,1	1	MR25	5322 116 50904
R 67	154K	1	MR25	5322 116 54714
R 71	4M	1	SPEC	5322 116 64025
R 72	681K	1	MR25	5322 116 55284
R 76	30,1	1	MR25	5322 116 50904
R 77	154K	1	MR25	5322 116 54714
R 81	4M	1	SPEC	5322 116 64025
R 82	681K	1	MR25	5322 116 55284
R 86	30,1	1	MR25	5322 116 50904
R 87	154K	1	MR25	5322 116 54714
R 91	2,26K	1	MR25	5322 116 50675
R 92	2,74K	1	MR25	5322 116 50636
R 93	2,26K	1	MR25	5322 116 50675
R 94	2,26K	1	MR25	5322 116 50675
R 96	562K	1	MR25	4822 116 51169
R 97	95,3K	1	MR25	5322 116 50567
R 200	10K	1	MR25	4822 116 51253
R 201	23,7K	1	MR25	5322 116 54646
R 202	1,21K	1	MR25	5322 116 54557
R 203	1K	1	MR25	5322 116 54549
R 204	220	20	0.5W	5322 101 14051
R 206	2,87K	1	MR25	5322 116 50414
R 207	2,74K	1	MR25	5322 116 50636
R 208	30,1	1	MR25	5322 116 50904
R 209	30,1	1	MR25	5322 116 50904
R 210	1M	1	MR30	5322 116 54188
R 211	8,2M	5	1W	5322 111 50345
R 212	10K	1	MR25	4822 116 51253

ITEM	OHM	TOL (%)	TYPE	ORDERING NUMBER
R 227	237	1	MR25	5322 116 50679
R 302	1M	1	MR30	5322 116 54188
R 303	100	1	MR25	5322 116 54469
R 304	75	1	MR25	5322 116 54459
R 306	75	1	MR25	5322 116 54459
R 307	191K	1	MR30	5322 116 55319
R 308	681K	1	MR30	5322 116 54263
R 309	845K	1	MR30	5322 116 55379
R 311	549K	1	MR30	5322 116 55139
R 312	205K	1	MR25	5322 116 54727
R 313	732K	1	MR30	5322 116 55321
R 314	806K	1	MR30	5322 116 55078
R 317	1M	1	MR30	5322 116 54188
R 318	90,9K	0,25	MR24C	5322 116 50859
R 319	8,25K	0,25	MR24C	5322 116 50979
R 354	487K	1	MR30	5322 116 55243
R 356	22K	20	0.5W	5322 101 14069
R 357	20,5K	1	MR25	5322 116 54643
R 358	22K	20	0.5W	5322 101 14069
R 359	20,5K	1	MR25	5322 116 54643
R 361	22K	20	0.5W	5322 101 14069
R 362	20,5K	1	MR25	5322 116 54643
R 363	8,25K	1	MR25	5322 116 54558
R 364	4,02K	1	MR25	5322 116 55448
R 365	5,11	1	MR25	5322 116 54192
R 366	2,49K	1	MR25	5322 116 50581
R 367	1,62K	1	MR25	5322 116 55359
R 368	5,11	1	MR25	5322 116 54192
R 369	1,62K	1	MR25	5322 116 55359
R 370	10	1	MR25	5322 116 50452
R 371	10	1	MR25	5322 116 50452
R 374	10	1	MR25	5322 116 50452
R 376	86,6K	1	MR25	5322 116 54692
R 377	51,1	1	MR25	5322 116 54442
R 402	1M	1	MR30	5322 116 54188
R 403	100	1	MR25	5322 116 54469
R 404	75	1	MR25	5322 116 54459
R 406	75	1	MR25	5322 116 54459
R 407	191K	1	MR30	5322 116 55319
R 408	681K	1	MR30	5322 116 54263
R 409	845K	1	MR30	5322 116 55379
R 411	549K	1	MR30	5322 116 55139
R 412	205K	1	MR25	5322 116 54727
R 413	732K	1	MR30	5322 116 55321
R 414	806K	1	MR30	5322 116 55078
R 417	1M	1	MR30	5322 116 54188
R 418	90,9K	0,25	MR24C	5322 116 50859
R 419	8,25K	0,25	MR24C	5322 116 50979
R 500	51,1	1	MR25	5322 116 54442
R 501	51,1	1	MR25	5322 116 54442
R 502	806K	1	MR30	5322 116 55078
R 503	12,7K	1	MR25	5322 116 50443
R 504	470	20	0,5W	5322 101 14047
R 506	12,7K	1	MR25	5322 116 50443
R 507	6,19K	1	MR25	5322 116 50608
R 508	6,49K	1	MR25	5322 116 54603
R 509	619	1	MR25	5322 116 54529
R 511	511	0,5	MR25	4822 116 51282
R 512	511	0,5	MR25	4822 116 51282
R 513	105	1	MR25	5322 116 54472
R 514	22K	20	0.5W	5322 101 14069
R 516	51.1K	1	MR25	5322 116 50672
R 517	5,9K	1	MR25	5322 116 50583
R 518	909	1	MR25	5322 116 55278
R 519	162	1	MR25	5322 116 50417

ITEM	OHM	TOL (%)	TYPE	ORDERING NUMBER
R 521	1K	20	0,5W	5322 100 10112
R 522	44,2	1	MR25	5322 116 50818
R 523	44,2	1	MR25	5322 116 50818
R 524	100	0,5	MR25	5322 116 55549
R 526	100	0,5	MR25	5322 116 55549
R 527	5,62K	0,5	MR25	4822 116 51281
R 528	909	0,5	MR25	5322 116 55278
R 529	51,1	1	MR25	5322 116 54442
R 531	51,1	1	MR25	5322 116 54442
R 532	909	0,5	MR25	5322 116 55278
R 533	5,62K	0,5	MR25	4822 116 51281
R 534	825	1	MR25	5322 116 54541
R 535	825	1	MR25	5322 116 54541
R 536	30,1	1	MR25	5322 116 50904
R 537	866	1	MR25	5322 116 54543
R 538	1,5K	5	0.5W	5322 116 34054
R 539	30,1	1	MR25	5322 116 50904
R 540	402	1	MR25	5322 116 54519
R 541	348	1	MR25	5322 116 54515
R 542	249	1	MR25	5322 116 54499
R 543	100	20	0,5W	5322 101 14011
R 546	909	1	MR25	5322 116 55278
R 547	220	20	0,5W	5322 101 14009
R 548	909	1	MR25	5322 116 55278
R 549	100	1	MR25	5322 116 54469
R 550	10	1	MR25	5322 116 50452
R 551	100	1	MR25	5322 116 54469
R 552	121	1	MR25	5322 116 54426
R 553	121	1	MR25	5322 116 54426
R 554	909	1	MR25	5322 116 55278
R 558	17,8K	1	MR25	5322 116 54637
R 559	5,11K	1	MR25	5322 116 54595
R 568	17,8K	1	MR25	5322 116 54637
R 569	5,9K	1	MR25	5322 116 50583
R 571	178	1	MR25	5322 116 54492
R 572	178	1	MR25	5322 116 54492
R 573	2,26K	1	MR25	5322 116 50675
R 577	100	1	MR25	5322 116 54469
R 581	4,99	1	MR25	5322 116 50568
R 582	4,99	1	MR25	5322 116 50568
R 583	4,99	1	MR25	5322 116 50568
R 584	4,99	1	MR25	5322 116 50568
R 586	4,99	1	MR25	5322 116 50568
R 587	4,99	1	MR25	5322 116 50568
R 600	51,1	1	MR25	5322 116 54442
R 601	51,1	1	MR25	5322 116 54442
R 602	806K	1	MR30	5322 116 55078
R 603	12,7K	1	MR25	5322 116 50443
R 604	470	20	0,5W	5322 101 14047
R 606	12,7K	1	MR25	5322 116 50443
R 607	6,19K	1	MR25	5322 116 50608
R 608	6,49K	1	MR25	5322 116 54603
R 609	619	1	MR25	5322 116 54529
R 611	511	0,5	MR25	4822 116 51282
R 612	511	0,5	MR25	4822 116 51282
R 613	105	1	MR25	5322 116 54472
R 614	22K	20	0.5W	5322 101 14069
R 616	51,1K	1	MR25	5322 116 50672
R 617	5,9K	1	MR25	5322 116 50583
R 618	909	1	MR25	5322 116 55278
R 619	162	1	MR25	5322 116 50417
R 621	1K	20	0,5W	5322 100 10112
R 622	44,2	1	MR25	5322 116 50818
R 623	44,2	1	MR25	5322 116 50818
R 624	100	0,5	MR25	5322 116 55549

ITEM	OHM	TOL (%)	TYPE	ORDERING NUMBER
R 626	100	0,5	MR25	5322 116 55549
R 627	5,62K	0,5	MR25	4822 116 51281
R 628	909	0,5	MR25	5322 116 55278
R 629	51,1	1	MR25	5322 116 54442
R 631	51,1	1	MR25	5322 116 54442
R 632	909	0,5	MR25	5322 116 55278
R 633	5,62K	0,5	MR25	4822 116 51281
R 634	825	1	MR25	5322 116 54541
R 635	825	1	MR25	5322 116 54541
R 636	30,1	1	MR25	5322 116 50904
R 637	866	1	MR25	5322 116 54543
R 638	1,5K	5	0.5W	5322 116 34054
R 639	30,1	1	MR25	5322 116 50904
R 640	402	1	MR25	5322 116 54519
R 641	158	0,5	MR25	5322 116 55418
R 646	953	1	MR25	5322 116 54547
R 647	100	20	0,5W	5322 101 14011
R 648	953	1	MR25	5322 116 54547
R 649	100	1	MR25	5322 116 54469
R 650	10	1	MR25	5322 116 50452
R 651	100	1	MR25	5322 116 54469
R 652	121	1	MR25	5322 116 54426
R 653	121	1	MR25	5322 116 54426
R 654	909	1	MR25	5322 116 55278
R 658	17,8K	1	MR25	5322 116 54637
R 659	5,11K	1	MR25	5322 116 54595
R 661	31,6K	1	MR25	5322 116 54657
R 662	17,8K	1	MR25	5322 116 54637
R 663	14K	1	MR25	5322 116 54629
R 664	8,25K	1	MR25	5322 116 54558
R 668	17,8K	1	MR25	5322 116 54637
R 669	5,9K	1	MR25	5322 116 50583
R 671	178	1	MR25	5322 116 54492
R 672	178	1	MR25	5322 116 54492
R 673	2,26K	1	MR25	5322 116 50675
R 674	47K	20	0,5W	5322 101 14043
R 676	33,2K	1	MR25	4822 116 51259
R 677	100	1	MR25	5322 116 54469
R 682	4,99	1	MR25	5322 116 50568
R 683	4,99	1	MR25	5322 116 50568
R 684	4,99	1	MR25	5322 116 50568
R 701	100	1	MR25	5322 116 54469
R 702	1,27K	1	MR25	5322 116 50555
R 703	750	1	MR25	4822 116 51234
R 704	402	1	MR25	5322 116 54519
R 705	4,99	1	MR25	5322 116 50568
R 706	1,27K	1	MR25	5322 116 50555
R 707	20,5K	1	MR25	5322 116 54643
R 708	6,81K	1	MR25	5322 116 54012
R 709	2,49K	1	MR25	5322 116 50581
R 710	4,99	1	MR25	5322 116 50568
R 711	2,49K	1	MR25	5322 116 50581
R 712	4,02K	1	MR25	5322 116 55448
R 713	4,02K	1	MR25	5322 116 55448
R 714	4,02K	1	MR25	5322 116 55448
R 716	4,02K	1	MR25	5322 116 55448
R 717	100	1	MR30	5322 116 54852
R 801	4,02K	1	MR25	5322 116 55448
R 802	8.25K	1	MR25	5322 116 54558
R 803	100	1	MR25	5322 116 54469
R 804	100	1	MR25	5322 116 54469
R 806	121	1	MR25	5322 116 54426
R 807	121	1	MR25	5322 116 54426
R 808	2,61K	1	MR25	5322 116 50671
R 809	1,33K	1	MR25	5322 116 54561

ITEM	OHM	TOL (%)	TYPE	ORDERING NUMBER
R 811	7,87K	1	MR25	5322 116 50458
R 812	4,7K	20	0.5W	5322 100 10114
R 813	10K	20	0,5W	5322 100 10113
R 814	2,2K	20	0.5W	5322 101 14008
R 816	30,1	1	MR25	5322 116 50904
R 817	100	20	0.05W	4822 100 10075
R 818	30,1	1	MR25	5322 116 50904
R 819	28,7	1	MR25	5322 116 54068
R 821	28,7	1	MR25	5322 116 54068
R 823	169	1	MR25	5322 116 54489
R 824	7,87K	1	MR25	5322 116 50458
R 825	4,99	1	MR25	5322 116 50568
R 826	2,26K	1	MR25	5322 116 50575
R 827	4,22K	1	MR25	5322 116 50729
R 828	68,1	1	MR25	5322 116 54455
R 829	68,1	1	MR25	5322 116 54455
R 831	56,2	1	MR25	5322 116 54446
R 832	56,2	1	MR25	5322 116 54446
R 833	909	1	MR25	5322 116 55278
R 837	909	1	MR25	5322 116 55278
R 838	1,21K	1	MR25	5322 116 54557
R 839	1,21K	1	MR25	5322 116 54557
R 843	681	1	MR25	4822 116 51233
R 847	90,9	1	MR25	5322 116 54466
R 848	100	20	0,5W	5322 101 14011
R 849	90,9	1	MR25	5322 116 54466
R 851	90,9	1	MR25	5322 116 54466
R 852	51,1	1	MR25	5322 116 54442
R 853	51,1	1	MR25	5322 116 54442
R 854	90,9	1	MR25	5322 116 54466
R 856	140	1	MR25	5322 116 54484
R 857	3,48K	1	MR25	5322 116 54585
R 858	3,01K	1	MR25	4822 116 51246
R 859	1,78K	1	MR25	5322 116 50515
R 861	1,78K	1	MR25	5322 116 50515
R 862	1,78K	1	MR25	5322 116 50515
R 863	1,78K	1	MR25	5322 116 50515
R 1001	205K	1	MR25	5322 116 54727
R 1002	51,1K	1	MR25	5322 116 50672
R 1003	51,1K	1	MR25	5322 116 50672
R 1004	205K	1	MR25	5322 116 54727
R 1006	3,65K	1	MR25	5322 116 54587
R 1007	8,25K	1	MR25	5322 116 54558
R 1008	301K	1	MR25	5322 116 54743
R 1009	511K	1	MR30	5322 116 54123
R 1011	4,02K	1	MR25	5322 116 55448
R 1013	12,7K	1	MR25	5322 116 50443
R 1014	470	20	0,5W	5322 101 14047
R 1016	12,7K	1	MR25	5322 116 50443
R 1017	2,87K	1	MR25	5322 116 50414
R 1018	562	1	MR25	5322 116 54009
R 1019	562	1	MR25	5322 116 54009
R 1021	3,65K	1	MR25	5322 116 54587
R 1022	1,54K	1	MR25	5322 116 50586
R 1023	1,54K	1	MR25	5322 116 50586
R 1024	30,1	1	MR25	5322 116 50904
R 1026	30,1	1	MR25	5322 116 50904
R 1027	619	1	MR25	5322 116 54529
R 1028	619	1	MR25	5322 116 54529
R 1029	10,5K	1	MR25	5322 116 50731
R 1031	4,02K	1	MR25	5322 116 55448
R 1032	12,1K	1	MR25	5322 116 50572
R 1033	1K	1	MR25	5322 116 54549
R 1034	16,2K	1	MR25	5322 116 55361
R 1036	3,65K	1	MR25	5322 116 54587

ITEM	OHM	TOL (%)	TYPE	ORDERING NUMBER
R 1037	8,25K	1	MR25	5322 116 54558
R 1038	2,61K	1	MR25	5322 116 50671
R 1039	1M	1	MR30	5322 116 54188
R 1041	22K	20	0.5W	5322 101 14069
R 1042	20,5K	1	MR25	5322 116 54643
R 1043	1,4K	1	MR25	5322 116 54562
R 1044	1,87K	1	MR25	5322 116 50728
R 1046	10K	1	MR25	4822 116 51253
R 1047	3,01K	1	MR25	4822 116 51246
R 1048	1M	1	MR30	5322 116 54188
R 1049	4,64K	1	MR25	5322 116 50484
R 1051	196K	1	MR25	5322 116 55364
R 1052	5,9K	1	MR25	5322 116 50583
R 1053	4,99	1	MR25	5322 116 50568
R 1054	4,99	1	MR25	5322 116 50568
R 1056	4,99	1	MR25	5322 116 50568
R 1202	48,7K	1	MR25	5322 116 50442
R 1203	3,48K	1	MR25	5322 116 54535
R 1204	6,19K	1	MR25	5322 116 50608
R 1207	10	1	MR25	5322 116 50452
R 1209	10K	1	MR25	4822 116 51253
R 1211	2,49K	1	MR25	5322 116 50581
R 1212	10K	1	MR25	4822 116 51253
R 1213	681	1	MR25	4822 116 51233
R 1214	5,11K	1	MR25	5322 116 54595
R 1216	1,05K	1	MR25	5322 116 54552
R 1217	7,87K	1	MR25	5322 116 50453
R 1218	32,4	0,5	MR25	5322 116 55421
R 1219	30,1	1	MR25	5322 116 50904
R 1220	9,09	1	MR25	5322 116 50863
R 1221	1,4K	1	MR25	5322 116 54562
R 1222	9,53K	1	MR25	5322 116 54617
R 1223	15,4K	1	MR25	5322 116 50479
R 1224	30,1	1	MR25	5322 116 50904
R 1226	1,54K	1	MR25	5322 116 50586
R 1227	7,5K	1	MR25	5322 116 54608
R 1228	7,87K	1	MR25	5322 116 50453
R 1229	37,4K	1	MR25	5322 116 54663
R 1230	26,1K	1	MR25	5322 116 54651
R 1231	33,2K	1	MR25	4822 116 51259
R 1232	22K	20	0.05W	4822 100 10051
R 1233	348	1	MR25	5322 116 54515
R 1234	2,26K	1	MR25	5322 116 50675
R 1236	21,5K	1	MR25	5322 116 50451
R 1237	4,99	1	MR25	5322 116 50568
R 1238	4,99	1	MR25	5322 116 50568
R 1239	4,99	1	MR25	5322 116 50568
R 1276	412K	0,5	MR25	5322 116 55424
R 1277	205K	0,5	MR25	5322 116 55387
R 1278	41,2K	0,5	MR25	5322 116 55423
R 1279	8,06K	0,5	MR25	5322 116 55428
R 1281	2K	0,5	MR25	4822 116 51243
R 1282	365	0,5	MR25	5322 116 55422
R 1283	412K	0,5	MR25	5322 116 55424
R 1284	82,5K	0,5	MR25	5322 116 55374
R 1286	20,5K	0,5	MR25	5322 116 55419
R 1287	4,02K	0,1	MR24E	5322 116 54283
R 1288	768	0,5	MR25	5322 116 55427
R 1289	6,19K	0,5	MR25	5322 116 55426
R 1290	953K	0,5	MR30	5322 116 55382
R 1291	261K	0,5	MR25	5322 116 54736
R 1401	3,16K	1	MR25	5322 116 50579
R 1402	51,1	1	MR25	5322 116 54442
R 1403	4,02K	1	MR25	5322 116 55448
R 1404	3,16K	1	MR25	5322 116 50579

ITEM	OHM	TOL (%)	TYPE	ORDERING NUMBER
R 1406	5,11K	1	MR25	5322 116 54595
R 1407	681	1	MR25	4822 116 51233
R 1408	8,25K	1	MR25	5322 116 54558
R 1409	3,01K	1	MR25	4822 116 51246
R 1411	9,09K	1	MR25	4822 116 51284
R 1412	2,37K	1	MR25	5322 116 54576
R 1414	3,01K	1	MR25	4822 116 51246
R 1416	3,32K	1	MR25	5322 116 54005
R 1417	1K	20	0,5W	5322 100 10112
R 1418	287	1	MR25	5322 116 54506
R 1419	100	20	0,5W	5322 101 14011
R 1421	8,66K	1	MR25	5322 116 54613
R 1422	16,2K	1	MR25	5322 116 55361
R 1423	20.5K	1	MR25	5322 116 54643
R 1424	36,5K	1	MR25	5322 116 50726
R 1425	100	1	MR25	5322 116 54469
R 1426	12,1K	1	MR25	5322 116 50572
R 1427	154K	1	MR25	5322 116 54714
R 1428	33,2K	1	MR25	4822 116 51259
R 1429	33,2K	1	MR25	4822 116 51259
R 1431	1K	1	MR25	5322 116 54549
R 1432	33,2K	1	MR25	4822 116 51259
R 1433	33,2K	1	MR25	4822 116 51259
R 1434	154K	1	MR25	5322 116 54714
R 1436	1,1K	1	MR25	4822 116 51236
R 1437	30,1	1	MR25	5322 116 50904
R 1438	3,01K	1	MR25	4822 116 51246
R 1439	30,1	1	MR25	5322 116 50904
R 1440	5,11K	1	MR25	5322 116 54595
R 1441	1,1K	1	MR25	4822 116 51236
R 1442	13,3K	1	MR25	5322 116 55276
R 1443	6,19K	1	MR25	5322 116 50608
R 1444	365K	1	MR30	5322 116 54762
R 1445	5,11K	1	MR25	5322 116 54595
R 1446	365K	1	MR30	5322 116 54762
R 1447	100	1	MR25	5322 116 54469
R 1448	100	1	MR25	5322 116 54469
R 1450	64,9K	1	MR25	5322 116 50514
R 1501	6,81K	1	MR25	5322 116 54012
R 1502	140	1	MR25	5322 116 54484
R 1503	3,48K	1	MR25	5322 116 54585
R 1506	162K	1	MR25	5322 116 54716
R 1507	3,48K	1	MR25	5322 116 54585
R 1509	11K	1	MR25	5322 116 54623
R 1511	51,1K	1	MR25	5322 116 50672
R 1512	6,19K	1	MR25	5322 116 50608
R 1513	26,1K	1	MR25	5322 116 54651
R 1514	6,19K	1	MR25	5322 116 50608
R 1516	22,6K	1	MR25	5322 116 50481
R 1517	2,05K	1	MR25	5322 116 50664
R 1518	511	1	MR25	4822 116 51282
R 1519	464	1	MR25	5322 116 50536
R 1521	226K	1	MR25	5322 116 54729
R 1522	680	5	0.5W	5322 116 34049
R 1523	4,02K	1	MR25	5322 116 55448
R 1524	100	1	MR25	5322 116 54469
R 1525	511	1	MR30	5322 116 54835
R 1526	64,9K	1	MR30	4822 116 51175
R 1527	17,8K	1	MR25	5322 116 54637
R 1528	33,2K	1	MR25	4822 116 51259
R 1529	4,87K	1	MR25	5322 116 50509
R 1531	11,5K	1	MR25	5322 116 55358
R 1532	1M	1	MR30	5322 116 54188
R 1533	100	1	MR25	5322 116 54469
R 1534	10K	20	0,5W	5322 100 10113

ITEM	OHM	TOL (%)	TYPE	ORDERING NUMBER
R 1535	1K	1	MR30	5322 116 54207
R 1536	4,64K	1	MR25	5322 116 50484
R 1537	1M	1	MR30	5322 116 54183
R 1538	1,2M	5	VR37	4822 110 42199
R 1539	2,2M	5	VR37	4822 110 42196
R 1541	5,6M	5	VR37	4822 110 42207
R 1542	78,7K	1	MR25	5322 116 50533
R 1543	100K	20	0.05W	4822 100 10072
R 1544	121K	1	MR25	5322 116 54704
R 1546	16,2K	1	MR25	5322 116 55361
R 1547	26,1K	1	MR25	5322 116 54651
R 1548	196K	1	MR25	5322 116 55364
R 1549	1M	20	0.05W	4822 100 10103
R 1551	383K	1	MR30	5322 116 54761
R 1552	4,99	1	MR25	5322 116 50568
R 1553	4,99	1	MR25	5322 116 50568
R 1554	4,99	1	MR25	5322 116 50568
R 1601	301	1	MR25	5322 116 54508
R 1602	12,1K	1	MR25	5322 116 50572
R 1603	2,05K	1	MR25	5322 116 50664
R 1604	10K	1	MR25	4822 116 51253
R 1606	681	1	MR25	4822 116 51233
R 1607	22K	20	0.5W	5322 101 14069
R 1608	38,3K	1	MR25	5322 116 55369
R 1609	953	1	MR25	5322 116 54547
R 1611	10K	1	MR25	4822 116 51253
R 1612	681	1	MR25	4822 116 51233
R 1613	6,19K	1	MR25	5322 116 50608
R 1614	3,48K	1	MR25	5322 116 54585
R 1616	2,05K	1	MR25	5322 116 50664
R 1617	301	1	MR25	5322 116 54508
R 1618	26,1K	1	MR25	5322 116 54651
R 1619	12,1K	1	MR25	5322 116 50572
R 2101	21,5K	1	MR25	5322 116 50451
R 2102	715	1	MR25	5322 116 50571
R 2103	21,5K	1	MR25	5322 116 50451
R 2104	196	1	MR25	5322 116 55273
R 2105	1,27K	1	MR25	5322 116 50555
R 2106	4,87K	1	MR25	5322 116 50509
R 2107	48,7K	1	MR25	5322 116 50442
R 2108	5,62K	1	MR25	4822 116 51281
R 2109	511	1	MR25	4822 116 51282
R 2111	2,15K	1	MR25	5322 116 50767
R 2112	7,5K	1	MR25	5322 116 54608
R 2113	332	1	MR25	4822 116 51226
R 2114	1K	1	MR25	5322 116 54549
R 2116	1,21K	1	MR25	5322 116 54557
R 2117	14,7K	1	MR25	5322 116 54632
R 2118	332	1	MR25	4822 116 51226
R 2119	21,5K	1	MR25	5322 116 50451
R 2121	1	1	MR25	4822 116 51179
R 2122	4,02K	1	MR25	5322 116 55448
R 2123	3,48K	1	MR25	5322 116 54585
R 2124	7,5K	1	MR25	5322 116 54608
R 2126	10K	1	MR25	4822 116 51253
R 2127	10K	1	MR25	4822 116 51253
R 2128	715	1	MR25	5322 116 50571
R 2129	33,2K	1	MR25	4822 116 51259
R 2131	750	1	MR25	4822 116 51234
R 2132	20K	1	MR25	5322 116 54642
R 2133	10K	1	MR25	4822 116 51253
R 2134	4,99K	1	MR25	5322 116 50523
R 2136	10K	1	MR25	4822 116 51253
R 2137	5,9K	1	MR25	5322 116 50583
R 2138	3,01K	1	MR25	4822 116 51246

ITEM	OHM	TOL (%)	TYPE	ORDERING NUMBER
R 2139	3,48K	1	MR25	5322 116 54585
R 2140	2,2K	20	0.75W	5322 100 10144
R 2141	16.9K	1	MR25	5322 116 54635
R 2142	226	1	MR25	5322 116 54497
R 2143	226	1	MR25	5322 116 54497
R 2144	30,1	1	MR25	5322 116 50904
R 2145	78,7	1	MR25	5322 116 50578
R 2147	1,62K	1	MR25	5322 116 55359
R 2148	10K	1	MR25	4822 116 51253
R 2149	100	1	MR25	5322 116 54469
R 2151	13,3K	1	MR25	5322 116 55276
R 2152	10K	2	7X0.2W	5322 111 94166
R 2153	33,2K	1	MR25	4822 116 51259
R 2154	4,42K	1	MR25	5322 116 50556
R 2156	511	1	MR25	4822 116 51282
R 2157	51,1	1	MR25	5322 116 54442
R 2158	133K	1	MR25	5322 116 54708
R 2159	1,47K	1	MR25	5322 116 50635
R 2161	15,4K	1	MR25	5322 116 50479
R 2162	422	1	MR25	5322 116 50459
R 2163	909	1	MR25	5322 116 55278
R 2164	1,69K	1	MR25	5322 116 54567
R 2166	21,5K	1	MR25	5322 116 50451
R 2167	4,99K	1	MR25	5322 116 50523
R 2168	10K	1	MR25	4822 116 51253
R 2169	20K	1	MR25	5322 116 54642
R 2171	1,15K	1	MR25	5322 116 50415
R 2172	4,87K	1	MR25	5322 116 50509
R 2173	48,7K	1	MR25	5322 116 50442
R 2174	5,62K	1	MR25	4822 116 51281
R 2176	1,27K	1	MR25	5322 116 50555
R 2177	1,62K	1	MR25	5322 116 55359
R 2178	196	1	MR25	5322 116 55273
R 2179	10K	1	MR25	4822 116 51253
R 2181	100	1	MR25	5322 116 54469
R 2301	7,15K	1	MR25	5322 116 54606
R 2302	3,32K	1	MR25	5322 116 54005
R 2307	10K	1	MR25	4822 116 51253
R 2308	5,11K	1	MR25	5322 116 54595
R 2309	10K	1	MR25	4822 116 51253
R 2311	10K	1	MR25	4822 116 51253
R 2312	1K	1	MR25	5322 116 54549
R 2313	5,11K	1	MR25	5322 116 54595
R 2314	10K	1	MR25	4822 116 51253
R 2316	40	15E	50V	4822 116 40001
R 2317	100	1	MR25	5322 116 54469
R 2319	40	15E	50V	4822 116 40001
R 2321	1,4K	1	MR25	5322 116 54562
R 2322	511	1	MR25	4822 116 51282
R 2323	1	1	MR25	4822 116 51179
R 2324	10K	1	MR25	4822 116 51253
R 2326	10K	1	MR25	4822 116 51253
R 2327	150	2	4X0.3W	5322 111 94258
R 2328	10K	2	7X0.2W	5322 111 94166
R 2329	21,5K	1	MR25	5322 116 50451
R 2331	22K	2	7X0.2W	5322 111 94191
R 2332	10K	1	MR25	4822 116 51253
R 2333	10K	1	MR25	4822 116 51253
R 2334	5,11K	1	MR25	5322 116 54595
R 2335	1K	1	MR25	5322 116 54549
R 2336	10K	1	MR25	4822 116 51253
R 2337	10K	1	MR25	4822 116 51253
R 2338	1	1	MR25	4822 116 51179
R 2339	10K	1	MR25	4822 116 51253
R 2340	1	1	MR25	4822 116 51179
R 2341	10K	2	7X0.2W	5322 111 94166

ITEM	OHM	TOL (%)	TYPE	ORDERING NUMBER
R 2342	150	2	4X0.3W	5322 111 94258
R 2343	150	2	4X0.3W	5322 111 94258
R 2344	150	2	4X0.3W	5322 111 94258
R 2345	51,1K	1	MR25	5322 116 50672
R 2346	150	2	4X0.3W	5322 111 94258
R 2347	10K	1	MR25	4822 116 51253
R 2348	11K	1	MR25	5322 116 54623
R 2349	5,11K	1	MR25	5322 116 54595
R 2351	100	1	MR25	5322 116 54469
R 2352	274	1	MR25	5322 116 54504
R 2353	10K	1	MR25	4822 116 51253
R 2354	365	1	MR25	5322 116 54516
R 2357	6,19K	1	MR25	5322 116 50608
R 2358	249K	1	MR25	5322 116 54386
R 2359	154	1	MR25	5322 116 50506
R 2361	110K	1	MR25	5322 116 54701
R 2362	22K	2	7X0.2W	5322 111 94191
R 2363	10K	1	MR25	4822 116 51253
R 2364	150	2	4X0.3W	5322 111 94258
R 2366	150	2	4X0.3W	5322 111 94258
R 2367	10K	2	7X0.2W	5322 111 94166
R 2369	1,47K	1	MR25	5322 116 50635
R 2372	3,48K	1	MR25	5322 116 54585
R 2373	6,19K	1	MR25	5322 116 50608
R 2376	301	1	MR25	5322 116 54508
R 2377	402	1	MR25	5322 116 54519
R 2378	48,7	1	MR25	5322 116 50511
R 2379	22K	2	7X0.2W	5322 111 94191
R 2380	10K	1	MR25	4822 116 51253
R 2381	1K	1	MR25	5322 116 54549
R 2382	1	1	MR25	4822 116 51179
R 2385	22K	2	7X0.2W	5322 111 94191
R 2386	10K	1	MR25	4822 116 51253
R 2387	21,5K	1	MR25	5322 116 50451
R 2388	150	2	4X0.3W	5322 111 94258
R 2389	150	2	4X0.3W	5322 111 94258
R 2391	150	2	4X0.3W	5322 111 94258
R 2392	10K	1	MR25	4822 116 51253
R 2393	487	1	MR25	5322 116 55451
R 2396	1	1	MR25	4822 116 51179
R 2397	150	2	4X0.3W	5322 111 94258
R 2398	150	2	4X0.3W	5322 111 94258
R 2399	10K	2	7X0.2W	5322 111 94166
R 2401	140	1	MR25	5322 116 54484
R 2410	2,26K	1	MR25	5322 116 50675
R 2441	12,7K	1	MR25	5322 116 50443
R 2442	511K	1	MR25	5322 116 55258
R 2443	12,7K	1	MR25	5322 116 50443
R 2444	51,1	1	MR25	5322 116 54442
R 2501	100	1	MR25	5322 116 54469
R 2502	1K	1	MR25	5322 116 54549
R 2503	100	1	MR25	5322 116 54469
R 2504	1,15K	1	MR25	5322 116 50415
R 2506	1,15K	1	MR25	5322 116 50415
R 2507	1,15K	1	MR25	5322 116 50415
R 2508	1,15K	1	MR25	5322 116 50415

Diodes

Type	Ordering number	Quantity PM 3542	PM 3543
AAZ 18	4822 130 30084	25	28
BAV 21	4822 130 30842	2	2
BAV 1	5322 130 34037	4	4
BAW 62	4822 130 30613	49	48
BAX 12	5322 130 34605	15	15
BA 182	5322 130 30644	18	18
BYX 49-300	5322 130 34558	1	1
BYX 55-35	4822 130 34275	2	2
BY 206	4822 130 30839	3	3
BY 225-200	4822 130 50312	1	1
BY 409A	5322 130 34594	6	6
BZX 61 - C110	5322 130 34671	1	1
BZX 75 - C2V8	4822 130 34048	2	2
BZX 75 - C3V6	4822 130 30765	2	2
BZX 79 - C11	4822 130 34488	1	1
BZX 79 - C3V0	4822 130 31251	2	2
BZX 79 - C36	4822 130 34368	3	3
BZX 79 - C5V1	4822 130 34233	4	4
BZX 79 - C5V6	4822 130 34173	1	1
BZX 79 - C6V8	4822 130 34278	1	1
BZX 79 - C75	4822 130 34685	1	1
BZX 79 - C9V1	4822 130 30862	2	2
BZX 87 - C6V2	5322 130 34067	1	1
OA 95	4822 130 30191	3	3

Transistors

Type	Ordering numbers	Quantity PM 3542	PM 3543
BC548C	4822 130 44196	34	34
BC549C	4822 130 44246	4	4
BC558B	4822 130 44197	16	16
BC559B	4822 130 44358	1	1
BDX77	5322 130 44899 (selected pair)	1	1
BD237	4822 130 44235	1	1
BFS21A	5322 130 40709	2	2
BFT45	5322 130 44603	2	2
BFQ10	5322 130 44355	1	1
BFQ13	5322 130 44404	8	8
BF199	4822 130 44154	6	6
BF324	4822 130 41448	4	4
BF338	4822 130 44108	2	2
BF450	4822 130 44237	12	12
BSS68	5322 130 44247	1	1
BSX20	5322 130 40417	3	3
ON561	5322 130 40709	1	1

Integrated circuits (PM 3542 - PM 3543)

Type	Ordering number	Quantity	
		PM 3542	PM 3543
AM9124CPC	5322 209 14863	4	4
HEF40174BP	5322 209 14444	1	1
HEF4029BP	5322 209 14057	4	5
HEF4042BP	5322 209 14071	2	2
HEF4050BP	5322 209 14068	1	1
LF357N	5322 209 80861	2	2
LM311N	5322 209 85503	1	1
NE5008N	5322 209 85791	2	2
NE521N	5322 209 14441	4	4
NE522N	5322 209 86462	1	1
N74LS00N	5322 209 84823	1	1
N74LS04N	5322 209 85486	7	10
N74LS05N	5322 209 84994	1	1
N74LS08N	5322 209 84995	2	2
N74LS132N	5322 209 85201	1	1
N74LS138N	5322 209 85647	1	1
N74LS153N	5322 209 85488	3	3
N74LS154N	5322 209 86085	1	1
N74LS156N	4822 209 80446	1	1
N74LS191N	5322 209 84989	5	5
N74LS21N	5322 209 85888	1	1
N74LS32N	5322 209 85311	5	6
N74LS74AN	5322 209 84986	1	1
N74S00N	5322 209 84167	5	5
N74S04N	5322 209 84475	1	1
N74S10N	5322 209 84954	2	2
N74S153N	5322 209 85688	1	1
N74S86N	5322 209 85452	3	3
AM27LS01PC	5322 209 50024	2	2
PROM-SET-(A and B) Programmed	5322 209 54693	-	1
PROM-SET (A and B) Programmed	5322 209 10144	1	-
CHARACTER GENERATOR	5322 209 10145	1	1
P8085 A	5322 209 86035	1	1
P8255 A	5322 209 86126	2	2
SL3145E	5322 130 34854	4	4
SN74LS123N-00	5322 209 85266	1	1
SN74LS151N-00	5322 209 86452	1	1
SN74LS240N-00	5322 209 85862	1	1
SN74LS244N-00	5322 209 86017	1	1
SN74LS257N-00	5322 209 80859	1	1
SN74LS279N-00	5322 209 85346	1	1
SN74LS373N-00	5322 209 86062	1	1
SN74LS374N-00	5322 209 85869	2	3
SN74S74N-00	5322 209 84183	4	4
93422 PC	5322 209 54673	4	6

7.3. Miscellaneous parts

Item	Ordering number	Designation
C.R.T.	5322 131 24029	Cathode Ray Tube (D14-125 GH/08)
B1	4822 130 31144	LED CQY24B/IV
B2301	5322 242 74364	Crystal 6 MC
E1	5322 134 44177	Lamp 28V - 80 mA
E2	5322 134 44177	Lamp 28V - 80 mA
F101	4822 252 20017	Thermal fuse for T101
F201	4822 253 30025	Fuse
F202	4822 253 30025	Fuse
K501	5322 280 24103	Reed relay
K601	5322 280 24103	Reed relay
K1401	5322 280 24103	Reed relay
K2101	5322 280 74139	Relay
K2102	5322 280 74139	Relay
L201	5322 281 64154	Coil
L202	5322 281 64154	Coil
L203	5322 281 64154	Coil
L801	5322 156 14074	Coil
L802	5322 156 14074	Coil
L1501	5322 150 14015	Rotary coil
L2001	5322 152 24092	Coil
S1-S2-S3	5322 276 84076	Push-button switch
S4		See item R3
S5		See item R4
S6	5322 273 74011	Attenuator switch without R7
S7		See item R7
S8	5322 273 74011	Attenuator switch without R8
S9		See item R8
S10	5322 273 84032	Time base switch without R9
S11		See item R9
S17		See item R11
S37	5322 277 14309	Tumbler switch 1-p 3 positions
S38	5322 277 14309	Tumbler switch 1-p 3 positions
S39	5322 277 14101	Tumbler switch 2-p 3 positions
S40	5322 276 14338	Push-button switch
T101	5322 146 34128	Mains transformer
T201	5322 158 34074	Coil assy
T203	5322 148 84047	Converter transformer

U2	5322 216 54299	Power supply board
U4	5322 218 64056	High voltage unit
U5	5322 216 54245	Amplifier board
U7	5322 320 44064	Delay line unit
U13	5322 216 51003	L.S. Analyzer board (PM 3542)
U13	5322 216 54297	L.S. Analyzer board (PM 3543)
U14	5322 216 54298	Interface oscilloscope board
U301	5322 216 54243	Attenuator unit
U302	5322 105 34034	Attenuator switch (R7,S6,S7,R8,S8,S9)
U303	5322 105 34059	Time base switch (R9,S10,S11)
U1302	5322 216 54301	Trigger Qual board
X1,	5322 264 24015	Calibration terminal
X2, X3	5322 267 10004	HF BNC Connector
X4	5322 535 84346	Earthing terminal
X5, X8, X10	5322 267 10004	HF BNC Connector
X7	4822 265 20051	DC input socket with switch
X11, X12	5322 265 44134	Connector 15-p
X13	5322 265 44134	Connector 15-p (only in PM 3543)
X14, X15	5322 264 24015	calibration terminal
X16	5322 264 61001	Connector 25-p
X2001	5322 264 54016	Male plug 6-p
X2002	5322 265 54006	Female plug 8-p
X2101,X2102,X2103	5322 268 14031	AMP Faston Pen
X2104	5322 268 24116	Coax socket
X2106	5322 268 14031	AMP Faston Pen
X2107	5322 265 54006	Female plug 4-p
X2108	5322 264 54016	Male plug 3-p
X2109	5322 265 54006	Female plug 3-p
X2111	5322 265 54006	Female plug 4-p
X2112, X2113	5322 265 54006	Female plug 10-p
X2114	5322 264 54016	Male plug 6-p
X2116	5322 264 54016	Male plug 8-p
X2117	5322 265 54006	Female plug 10-p
X2118	5322 265 54006	Female plug 6-p
X2201, X2202	5322 267 54149	Female plug 20-p
X2203	5322 264 54016	Male plug 4-p
X2208	5322 265 54006	Female plug 4-p
X2301	5322 267 64031	Connector 10-p
X2302, X2303	5322 268 24116	Coax socket
X2304, X2306	5322 290 34123	Solder tag
X2308, X2309	5322 267 64031	Connector 10-p
X2311	5322 267 64031	Connector 12-p
X2313	5322 268 24116	Coax socket
X2314, X2316	5322 267 64031	Connector 10-p
X2317, X2318	5322 267 64031	Connector 20-p
X2319	5322 264 54016	Male plug 10-p
X2441, X2501	5322 268 24116	Coax socket
X2502	5322 267 64027	Connector 6-p
.....	5322 268 14141	Contact pin for X2104, X2302, X 2303, X 2313, X 2441, X2501

NOTES:

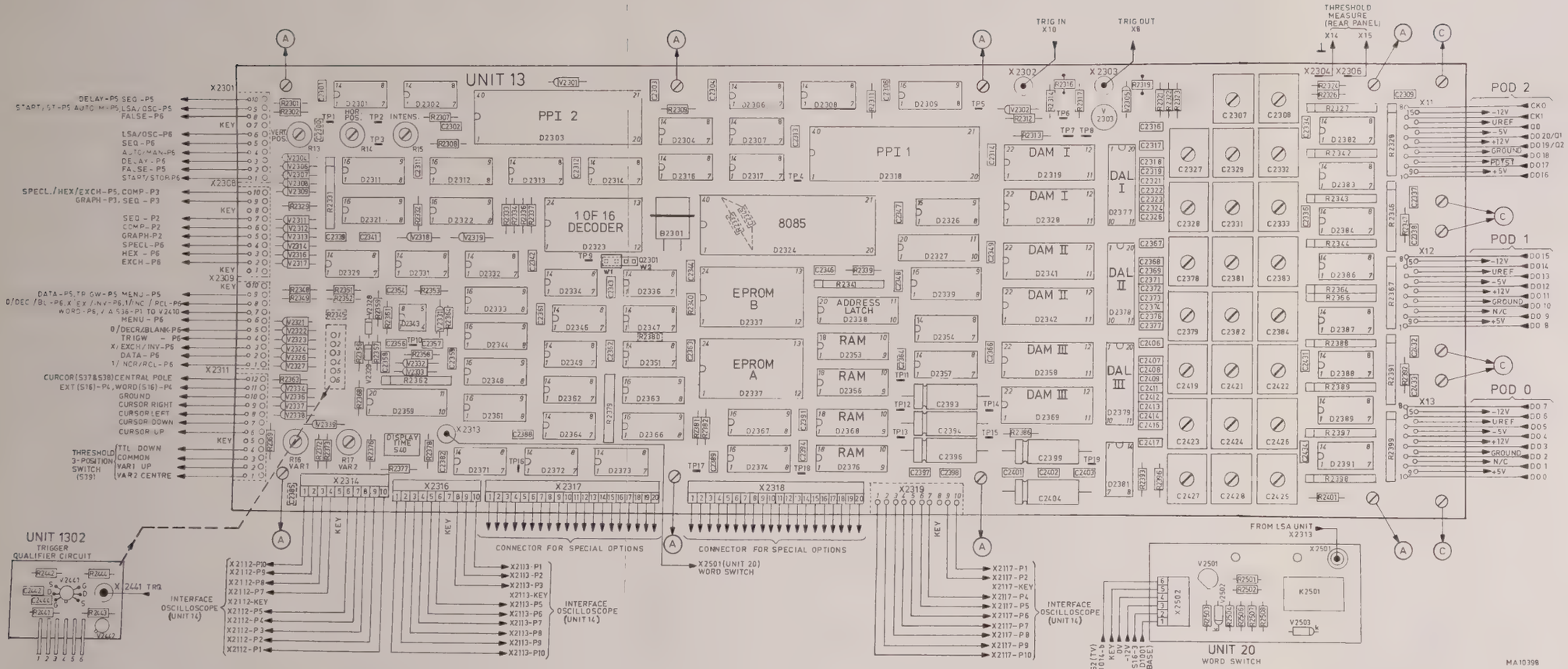


Fig. 7.4. L.S. Analyzer board

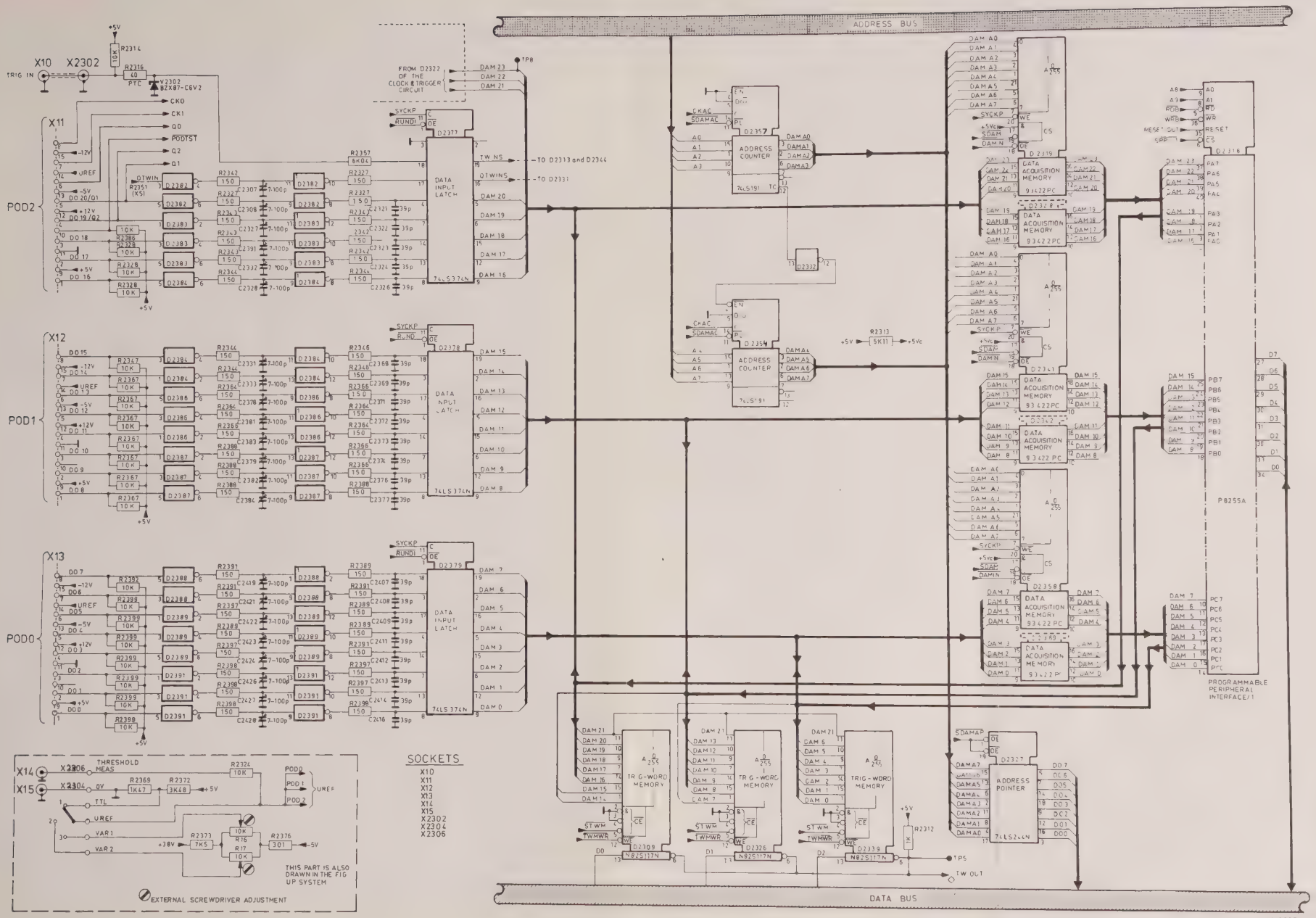


Fig. 7.5. Data Acquisition circuit

NOTES:

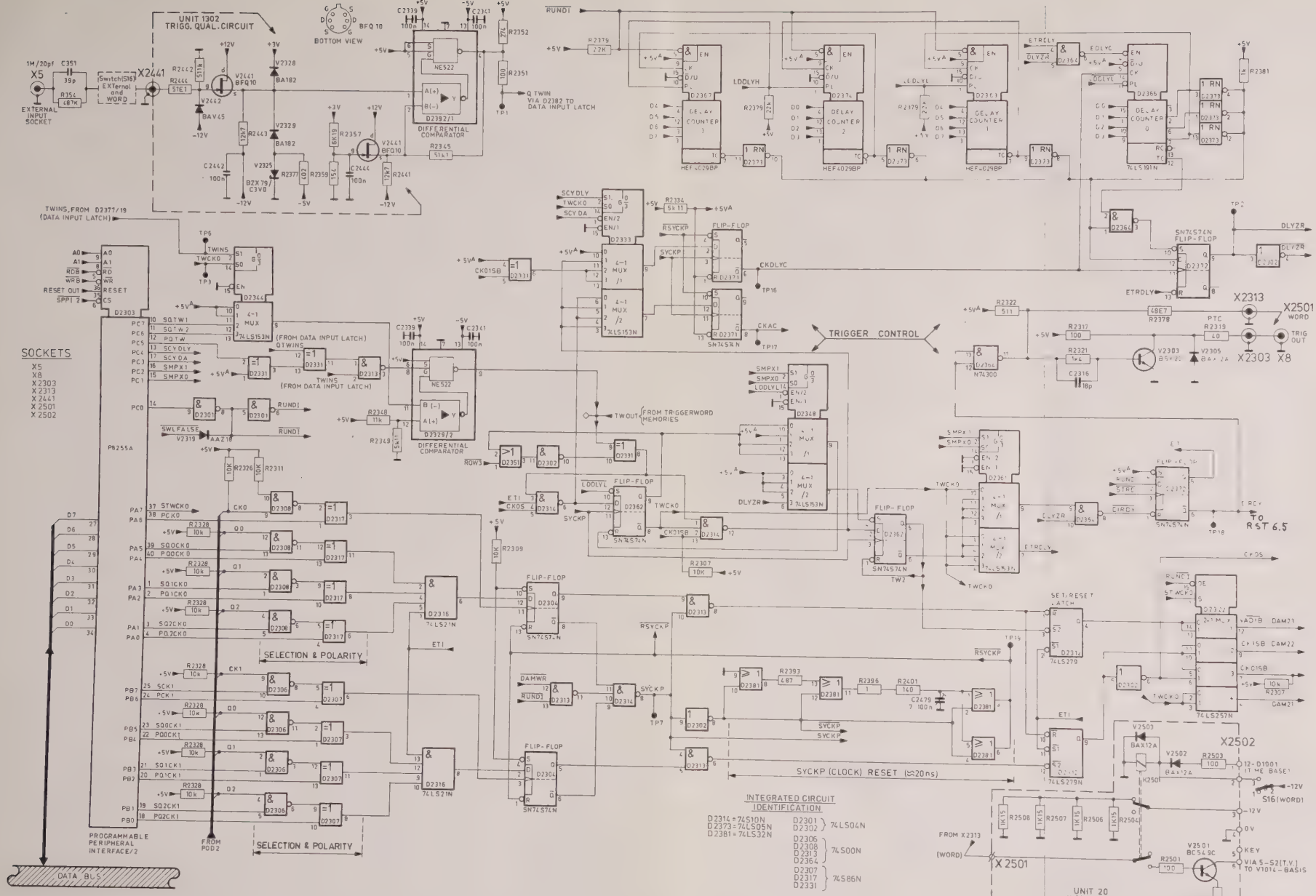


Fig. 7.6. Clock, Qualifier and Triggercontrol circuit

NOTES:

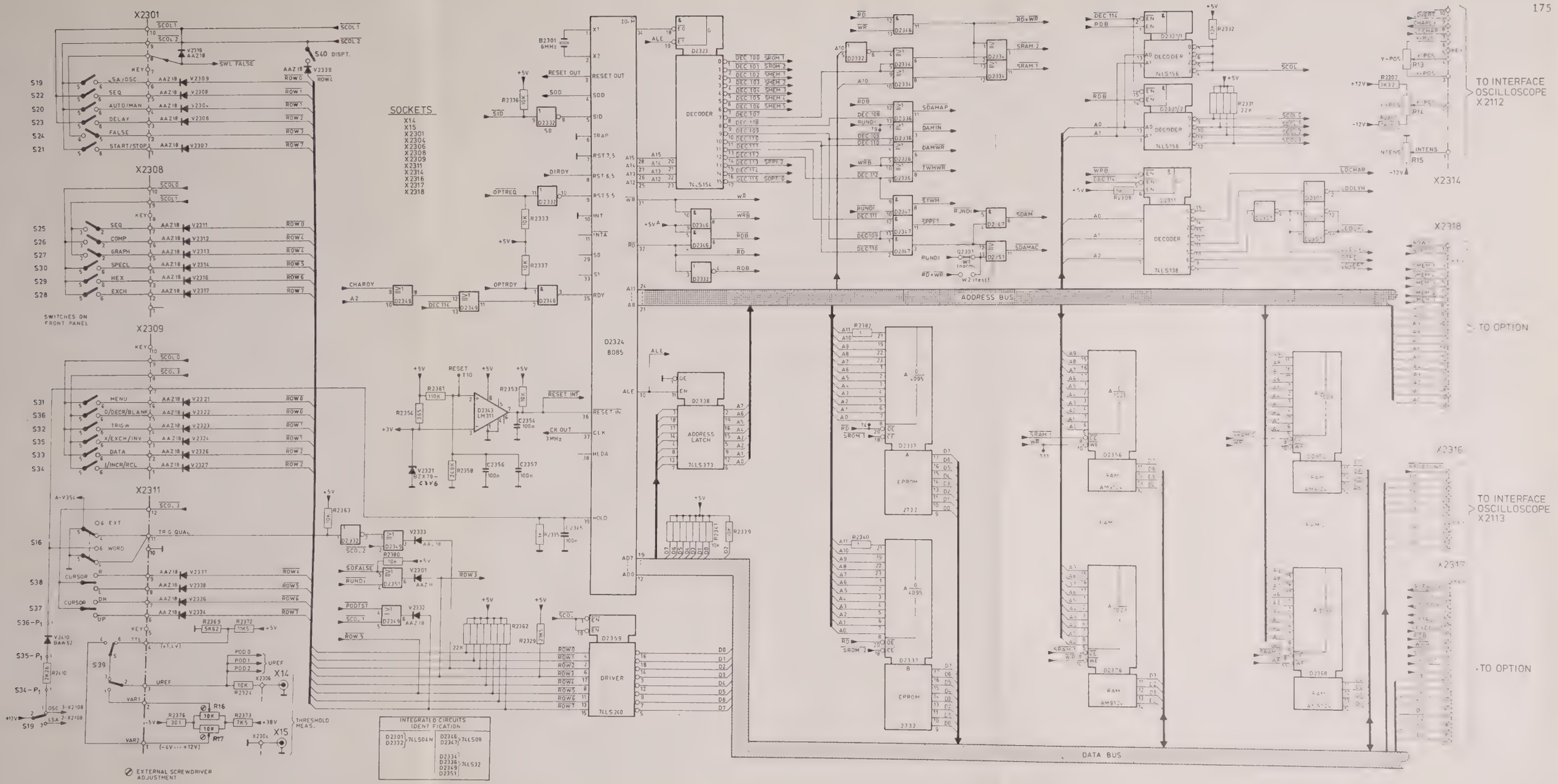


Fig. 7.7. Microprocessor system

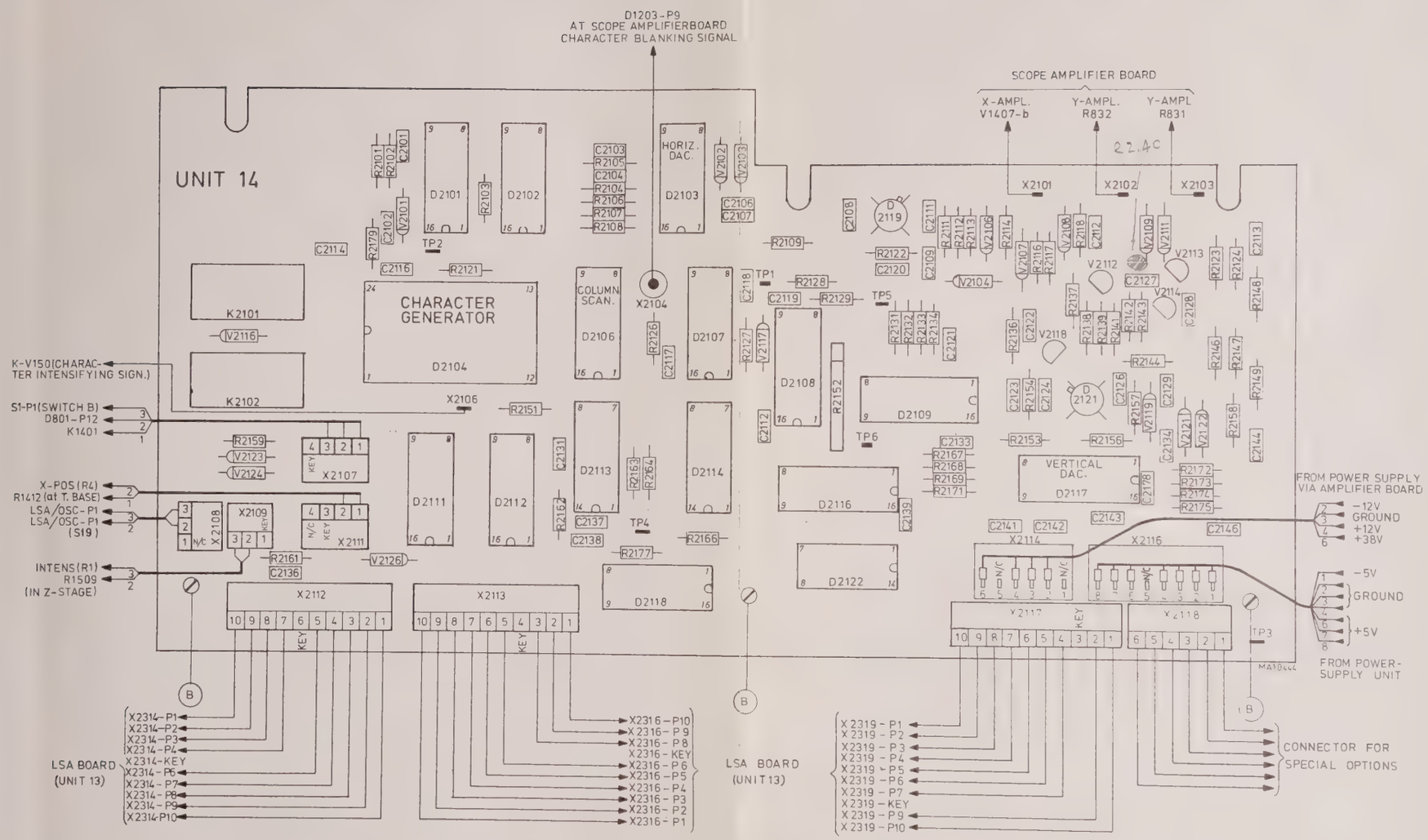


Fig. 7.8. Interface oscilloscope board

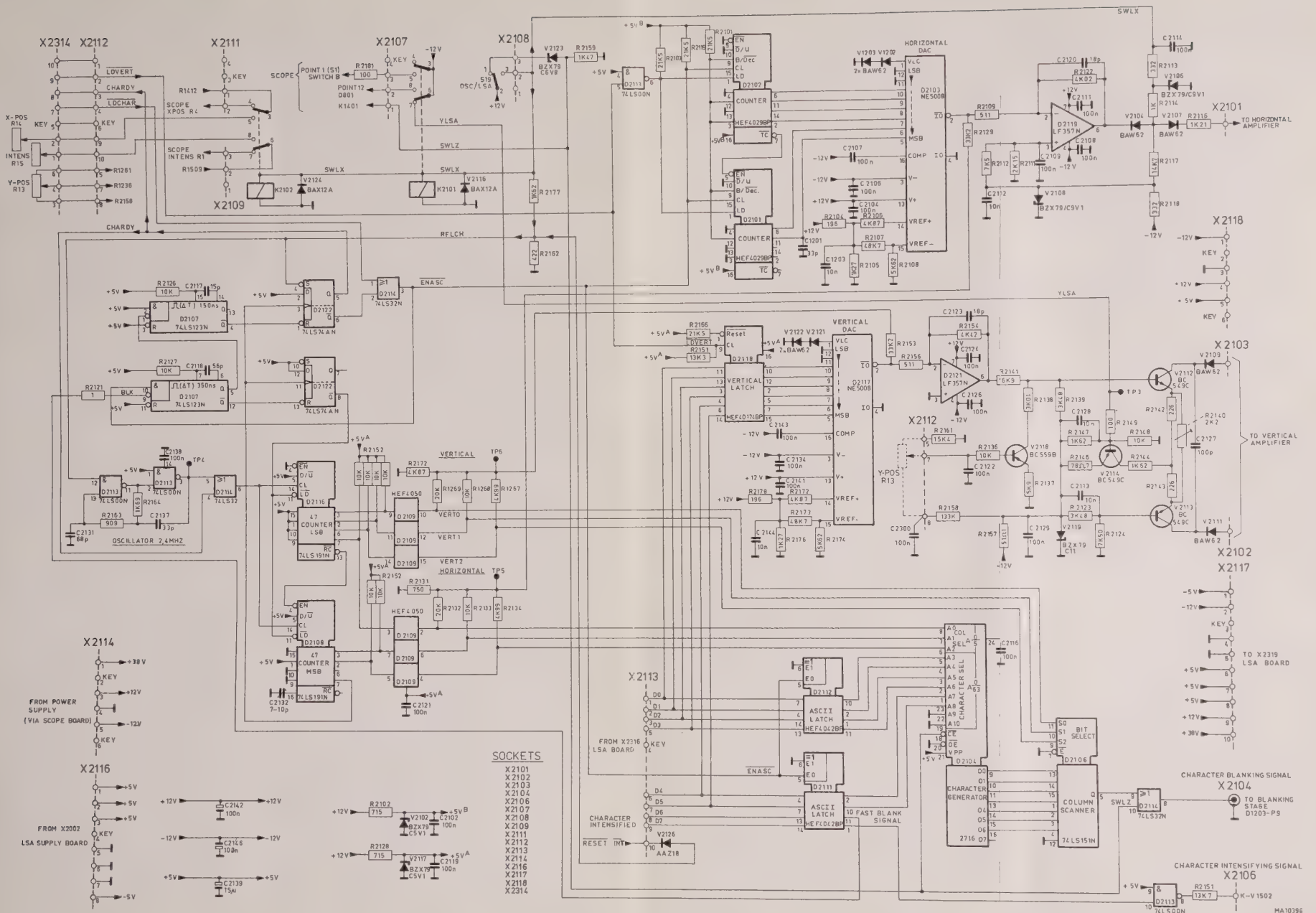
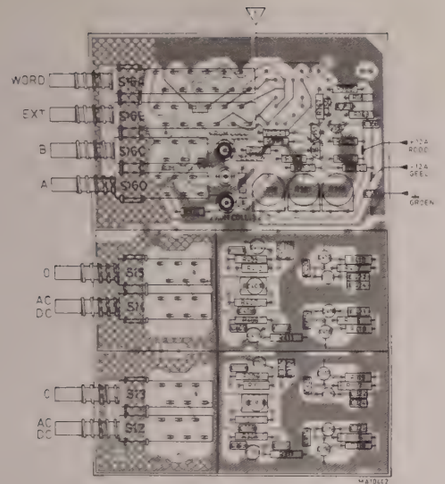


Fig. 7.9. Interface oscilloscope circuit

NOTES:

LOCATION LIST (of components on the amplifier board)

Item	Grid Loc.
C101	Rear panel
C200	Power supply
C201	Power supply
C202	Power supply
C203	Power supply
C204	Power supply
C206	Power supply
C207	Power supply
C208	Power supply
C209	Power supply
C211	Power supply
C212	High tension unit
C213	High tension unit
C214	High tension unit
C216	High tension unit
C217	High tension unit
C218	Power supply
C219	Power supply
C221	Power supply
C222	Power supply
C223	Power supply
C224	Power supply
C226	Power supply
C227	Power supply
C228	Power supply
C229	Power supply
C231	Power supply
C301	Att. unit
C305	Att. unit
C307	Att. unit
C308	Att. unit
C309	Att. unit
C310	Att. unit
C311	Att. unit
C312	Att. unit
C313	Att. unit
C314	Att. unit
C315	Att. unit
C316	Att. unit
C317	Att. unit
C318	Att. unit
C319	Att. unit
C320	Att. unit
C321	Att. unit
C322	Att. unit
C324	Att. unit
C351	Att. unit
C352	Att. unit
C353	Att. unit
C354	Att. unit
C356	Att. unit
C357	Att. unit
C358	Att. unit
C401	Att. unit
C405	Att. unit
C407	Att. unit
C408	Att. unit
C409	Att. unit
C410	Att. unit
C411	Att. unit
C412	Att. unit
C413	Att. unit
C414	Att. unit
C415	Att. unit
C416	Att. unit
C417	Att. unit
C418	Att. unit
C419	Att. unit
C420	Att. unit
C421	Att. unit
C422	Att. unit
C424	Att. unit
C501	C-2
C502	C-2
C504	D-2
C507	D-2
C508	D-2
C509	D-2
C511	D-2
C512	E-2
C513	E-2
C514	E-2
C517	E-2
C518	E-2
C519	E-2
C521	D-2
C522	E-2
C523	C-2
C524	B-3
C526	C-2
C527	B-2/C-2
C528	D-3
C529	B-2
C531	C-2
C601	C-3
C602	C-3
C604	D-3
C607	D-2/D-3
C608	D-3
C609	D-2
C611	D-3
C612	D-3
C613	D-3
C614	D-3
C616	E-3
C617	E-3
C618	E-3
C619	E-3
C621	E-3
C622	E-2/E-3
C623	C-3
C627	B-2/C-2
C629	B-3
C631	C-3
C701	D-2
C702	E-2
C703	E-2
C704	E-2
C705	E-2
C706	D-2
C707	E-2
C801	E-3
C802	E-3
C803	E-3
C804	F-3
C805	F-2
C806	F-3
C807	E-3
C808	F-3
C809	F-3
C810	F-2
C811	F-3
C813	F-3
C814	F-2
C815	F-3
C816	F-2
C818	F-2
C819	F-2
C821	F-2
C1001	C-3/C-4
C1002	C-4
C1003	B-4
C1004	B-3
C1006	C-3/C-4
C1007	C-4
C1008	C-4
C1011	C-4
C1012	C-4
C1013	B-4
C1016	C-3/C-4
C1017	C-4
C1018	C-3/C-4
C1019	C-4
C1201	D-3
C1202	D-4
C1203	D-3
C1204	D-3/D-4
C1205	D-4
C1206	C-4
C1207	D-3/D-4
C1208	E-3/E-4
C1209	D-3/D-4
C1210	C-4
C1211	C-4
C1212	C-3
C1213	E-4
C1214	E-4
C1216	E-3/E-4
C1401	E-4
C1402	E-4
C1403	E-4
C1404	F-3
C1406	G-3
C1407	F-3/G-3
C1408	F-3
C1409	F-3/G-3
C1411	F-2/G-2
C1412	F-2/G-2
C1413	F-2/G-2
C1414	G-3
C1416	G-2
C1417	G-2
C1418	G-2
C1419	F-3
C1421	F-2
C1501	E-4
C1502	F-4
C1503	F-4
C1504	. .
C1506	F-4
C1507	F-4
C1508	F-4
C1509	F-4/G-4
C1511	F-4
C1512	F-4/G-4
C1513	On Tube
C1601	B-2
C1602	A-2
R1	Front panel
R2	Front panel
R3	Front panel
R4	Front panel
R5	Front panel
R6	Front panel
R7	Front panel
R8	Front panel
R9	Front panel
R10	Front panel
R11	Front panel
R200	Power supply
R201	Power supply
R202	Power supply
R203	Power supply
R204	Power supply
R206	Power supply
R207	Power supply
R208	Power supply
R209	Power supply
R210	Power supply
R211	High t. u.
R212	Power supply
R227	B-3
R302	Att. unit
R303	On switch S6
R304	On switch S6
R306	On switch S6
R307	Att. unit
R308	Att. unit
R309	Att. unit
R311	Att. unit
R312	Att. unit
R313	On switch S6
R314	On switch S6
R316	Att. unit
R317	Att. unit
R318	Att. unit
R319	Att. unit
R354	Att. unit
R356	Att. unit
R357	Att. unit
R358	Att. unit
R359	Att. unit
R361	Att. unit
R362	Att. unit
R363	Att. unit
R364	Att. unit
R366	Att. unit
R367	Att. unit
R369	Att. unit
R371	Att. unit
R372	Att. unit
R373	Att. unit
R402	Att. unit
R403	On switch S8
R404	On switch S8
R406	On switch S8
R407	Att. unit
R408	Att. unit
R409	Att. unit
R411	Att. unit
R412	Att. unit
R413	On switch S8
R414	On switch S8
R416	Att. unit
R417	Att. unit
R418	Att. unit
R419	Att. unit
R500	C-2
R501	B-2/C-2
R502	B-2/C-2
R503	C-2
R504	B-2/C-2
R506	B-2
R507	C-2
R508	C-2
R509	C-2
R511	C-2
R512	C-2
R513	C-2
R514	C-2
R516	C-2
R517	C-2
R518	C-2
R519	C-2
R521	C-2/D-2
R522	C-2/D-2
R523	C-2/D-2
R524	D-2
R526	C-2/D-2
R527	C-2/D-2
R528	C-2
R529	C-2/D-2
R531	C-2/D-2
R532	D-2
R533	D-2
R534	D-2
R536	D-2
R537	D-2
R538	D-2
R539	D-2
R541	D-2
R542	D-2
R543	D-2
R544	D-2
R546	D-2
R547	D-2
R548	D-2
R549	D-2
R550	D-2
R551	D-2
R552	D-2
R553	D-2
R554	D-2
R556	E-2
R557	E-2
R558	E-2
R559	E-2
R567	E-2
R568	E-2
R569	E-2
R571	E-2
R572	E-2
R573	D-2
R577	E-2
R581	B-3
R582	B-2
R583	B-2
R584	C-2
R586	D-3
R587	D-3
R600	C-3
R601	B-3/C-3
R602	B-3/C-3
R603	C-3
R604	B-3/C-3
R606	B-3
R607	C-3
R608	C-3
R609	C-3
R611	C-3
R612	C-3
R613	C-3
R614	C-3
R616	C-3
R617	C-2
R618	C-3
R619	C-2/C-3
R621	C-3/D-3
R622	C-3/D-3
R623	C-3/D-3
R624	D-3
R626	C-3/D-3
R627	C-3/D-3
R628	C-3
R629	C-3/D-3
R631	C-3/D-3
R632	D-3
R633	D-3
R634	D-3
R636	D-3
R637	D-3
R638	D-3
R639	D-3
R641	D-3
R644	D-3
R646	D-3
R647	D-2/D-3
R648	D-3
R649	D-2/D-3
R650	D-2
R651	D-2/D-3
R652	D-2/D-3
R653	D-2/D-3
R654	D-2/D-3
R656	D-3
R657	D-3
R658	D-3
R659	E-3
R661	E-3
R662	E-3
R663	E-3
R664	E-3
R666	E-3
R667	E-3
R668	E-3
R669	E-3
R671	E-3
R672	E-3
R673	E-3
R674	D-3
R676	D-3
R677	E-2
R682	B-3
R683	B-3
R684	C-3
R701	D-2
R702	E-2
R703	E-2
R704	E-2
R705	E-3
R706	D-2/E-2
R707	D-2
R708	D-2
R709	E-2
R710	D-3
R711	E-2/E-3
R712	E-2
R713	E-3
R714	E-2
R716	E-2/E-3
R717	E-3
R801	E-2
R802	E-3
R803	E-2/E-3
R804	E-2
R806	E-3
R807	E-3
R808	E-2
R809	E-2
R811	E-3/F-3
R812	F-3
R813	F-3
R814	E-3
R816	E-2/E-3
R817	F-3
R818	E-2
R819	F-3
R821	F-3
R822	F-3
R823	F-3
R824	F-2/F-3
R825	F-3
R826	F-2/F-3
R827	F-3
R828	F-3
R829	F-3
R831	F-2
R832	F-2
R833	F-2
R837	F-2
R838	F-2
R839	F-2
R841	F-2
R842	F-2
R843	F-2
R844	F-2
R846	F-2
R847	F-2
R848	F-2
R849	F-2
R851	F-2
R852	F-2
R853	F-2
R854	E-2
R856	E-2
R857	E-2
R858	E-2/F-2
R859	F-2
R861	E-2
R862	F-2
R863	E-2
R1001	C-3
R1002	C-3
R1003	C-4
R1004	C-4
R1005	B-4
R1006	B-4
R1007	B-4
R1008	C-4
R1009	B-4
R1011	B-4
R1012	B-3
R1013	B-3
R1014	B-3
R1016	B-3
R1017	B-4
R1018	B-4
R1019	B-4
R1021	B-4
R1022	C-4
R1023	C-3
R1024	B-4
R1026	B-4
R1027	B-4
R1028	B-4
R1029	B-4
R1031	B-4
R1032	B-4/C-4
R1033	B-4
R1034	B-4
R1036	B-4
R1037	B-4
R1038	B-4
R1039	C-4
R1041	C-4
R1042	C-4
R1043	C-4
R1044	C-4
R1046	C-4
R1047	C-4
R1048	C-4
R1049	B-4
R1051	C-4
R1052	B-4
R1053	C-3
R1054	C-3
R1056	C-3
R1201	D-3
R1202	D-4
R1203	D-4
R1204	D-4
R1207	D-4
R1208	D-4
R1209	D-4
R1211	D-4
R1212	D-4
R1213	D-3
R1214	C-3
R1216	D-4
R1217	D-4
R1218	D-4
R1219	D-4
R1221	D-4
R1222	D-4
R1223	D-4
R1224	D-3/D-4
R1226	D-3/D-4
R1227	D-4
R1228	E-3/E-4
R1229	D-4
R1231	D-4
R1232	E-4
R1233	E-4
R1234	E-4
R1236	D-4
R1237	E-3
R1238	E-3
R1239	E-3
R1276	On switch S10
R1277	On switch S10
R1278	On switch S10
R1279	On switch S10
R1281	On switch S10
R1282	On switch S10
R1283	On switch S10
R1284	On switch S10
R1286	On switch S10
R1287	On switch S10
R1288	On switch S10
R1289	On switch S10
R1401	E-4
R1402	E-4
R1403	E-4
R1404	E-4
R1406	E-4
R1407	E-4
R1408	E-4
R1409	E-4
R1411	E-4
R1412	E-4
R1414	E-4
R1416	E-4
R1417	E-4
R1418	E-4
R1419	E-3
R1421	E-4
R1422	E-4
R1423	E-4
R1424	G-3
R1425	F-3
R1426	F-3
R1427	F-2
R1428	F-3
R1429	F-3
R1431	F-3
R1432	G-3
R1433	G-3
R1434	G-2
R1436	F-2
R1437	F-3
R1438	G-3
R1439	G-3
R1440	On R4
R1441	G-2
R1442	F-3
R1443	G-3
R1444	G-2
R1445	On R4
R1446	G-2
R1447	G-3
R1448	F-3
R1450	On R4
R1501	E-3
R1502	F-3
R1503	E-4
R1506	F-4
R1507	F-4
R1508	F-4
R1509	F-4
R1511	F-4
R1512	F-4
R1513	F-4
R1514	F-4
R1516	F-4
R1517	F-4
R1518	F-4
R1519	F-4
R1521	F-4
R1522	F-4
R1523	F-4
R1524	F-4
R1525	F-4
R1526	F-4
R1527	F-4
R1528	F-4
R1529	F-4
R1531	F-4
R1532	G-4
R1533	F-4
R1534	F-4
R1535	On tube
R1536	On tube
R1537	G-4
R1538	Power supply
R1539	Power supply
R1541	Power supply
R1542	Power supply
R1543	Power supply
R1544	Power supply
R1546	Power supply
R1547	Power supply
R1548	Power supply
R1549	Power supply
R1551	Power supply
R1552	F-3/F-4
R1553	F-3
R1554	F-3/F-4
R1601	B-2
R1602	B-2
R1603	B-2
R1604	B-2
R1606	B-2
R1607	B-2
R1608	B-2
R1609	B-2
R1611	B-2
R1612	B-2
R1613	B-2
R1614	B-2
R1616	B-2
R1617	B-2
R1618	A-2
R1619	A-2
V1	Tube
V201	Power supply
V202	Power supply
V203	Power supply
V204	Power supply
V206	Power supply
V207	Power supply
V208	Power supply
V209	Power supply
V211	Power supply
V212	Power supply
V213	Power supply
V214	Power supply
V216	Power supply
V217	Power supply
V218	Power supply
V219	Power supply
V221	Power supply
V222	Power supply
V223	Power supply
V224	Power supply
V226	High tension unit
V227	High tension unit
V228	High tension unit
V229	High tension unit
V231	High tension unit
V232	Power supply
V233	Power supply
V234	Power supply
V236	Power supply
V237	Power supply
V238	Power supply
V239	Power supply
V241	Power supply
V242	Power supply
V243	Power supply
V244	Power supply
V246	Power supply
V247	Power supply
V351	Att. unit
V352	Att. unit
V353	Att. unit
V354	Att. unit
V501	C-2
V504	B-2/C-2
V506	D-2
V507	D-2
V508	D-2/E-2
V509	D-2/E-2
V511	D-2
V512	D-2
V513	E-2
V514	E-2
V518	E-2
V519	E-2
V521	E-2
V522	E-2
V523	E-2
V524	E-2
V526	E-2
V601	C-3
V604	B-3/C-3
V606	D-3
V607	D-3
V608	D-3
V609	D-3
V611	D-2/D-3
V612	D-3
V613	D-3/E-3
V614	E-3
V616	E-3
V617	E-3
V618	E-3
V619	E-3
V621	E-3
V622	E-3
V623	E-3
V624	E-3
V626	E-3
V701	E-2
V702	E-2
V703	E-2
V704	E-2
V801	E-2
V802	F-3
V803	F-2
V804	F-2
V806	F-2
V807	F-2
V808	F-2
V809	E-2
V1001	C-3/C-4
V1002	C-4
V1003	B-4
V1004	B-4
V1006	B-3/C-3
V1008	B-4/C-4
V1009	B-4
V1011	B-4
V1012	B-4
V1013	C-4
V1014	C-4
V1016	C-4
V1017	B-4
V1201	D-3
V1202	D-4
V1203	D-4
V1204	D-4
V1206	D-4
V1207	D-4
V1208	D-4
V1209	D-4
V1211	D-4
V1212	D-4
V1213	D-4
V1214	D-4/E-4
V1216	D-3
V1217	D-3/E-3
V1218	E-4
V1219	D-4
V1221	D-4
V1222	D-3/D-4
V1223	E-3
V1401	E-4
V1402	E-4
V1403	E-4
V1404	E-4
V1406	E-4
V1407	E-4
V1408	E-4
V1409	E-4
V1411	E-4
V1412	F-2
V1413	F-2
V1414	F-2
V1416	F-3/G-3
V1417	F-3
V1419	G-3
V1421	G-3
V1422	G-2
V1423	G-2
V1424	G-2
V1426	G-2
V1427	G-2
V1428	G-2
V1501	D-4
V1502	E-4
V1503	E-4
V1504	F-4
V1506	F-3
V1508	E-4
V1511	F-4
V1512	F-4
V1513	F-4
V1514	F-4
V1516	F-4
V1517	F-4
V1518	F-4
V1519	G-4
V1521	B-2
V1522	B-2
V1601	B-2
V1602	B-2
V1603	B-2
V1604	B-2
D501	C-2
D601	C-3
D801	F-2/F-3
D802	Delay line
D1001	B-4
D1201	C-4/D-4
D1202	C-4/D-4
D1203	C-4/D-4
B1	LED
F201	Power supply
K501	C-2
K601	C-3
K1401	E-3
L201	Power supply
L202	Power supply
L203	Power supply
L801	F-2
L802	F-2
L1501	Trace rot. coil
T101	Rear panel
T201	Power supply
T202	Power supply


WORD
EXT
B
A
S60
S61
S62
S63
S64
S65
S66
S67
S68
S69
S70
S71
S72
S73
S74
S75
S76
S77
S78
S79
S80
S81
S82
S83
S84
S85
S86
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S88
S89
S90
S91
S92
S93
S94
S95
S96
S97
S98
S99

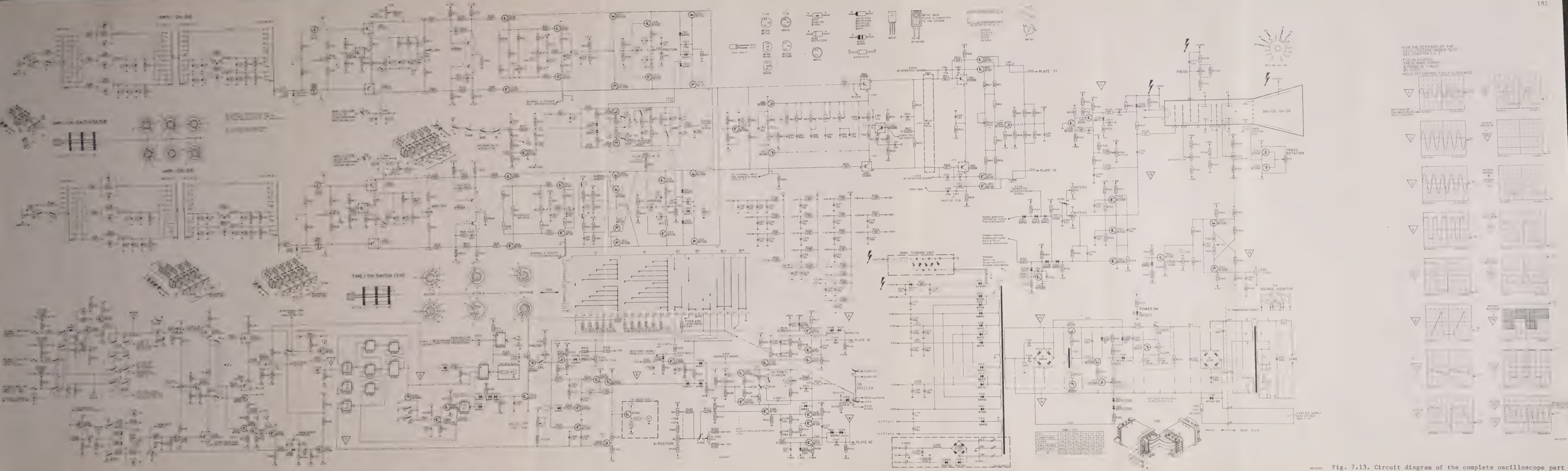

Fig. 7.13. Circuit diagram of the complete oscilloscope part

8.PM 3542 INFORMATION

8.1.General information

In this Chapter you will find the drawings which concern the PM 3542.
The PM 3542 hardware differs from the PM 3543 only in the data acquisition circuit. (see also block diagram PM 3542).
Differences in for example "Circuit Description", "Checking and Adjusting" are mentioned in the relevant Chapter of this Manual.
Due to the great difference in the EPROM contents of the PM 3542 and PM 3543, the PM 3542 PROM-set ordering number is different (See Chapter "Parts List").

Note : Service testprogram.
In the service testprogram of the PM 3542 the decoder tests (test 2, 3 and 4) are left out.

The sequence of the program as shown in the figure "Memory Map" (Fig. 25) is het same for both instruments.

8.2.Hardware differences

The components listed below are not present in the PM 3542.

R2389	C2407	C2419	D2339
R2391	C2408	R2421	D2358
R2397	C2409	C2422	D2369
R2398	C2411	C2423	D2379
R2399	C2412	C2424	D2388
	C2413	C2426	D2389
	C2414	C2427	D2391
	C2416	C2428	

See also Chapter 7 "Parts list".

NOTES:

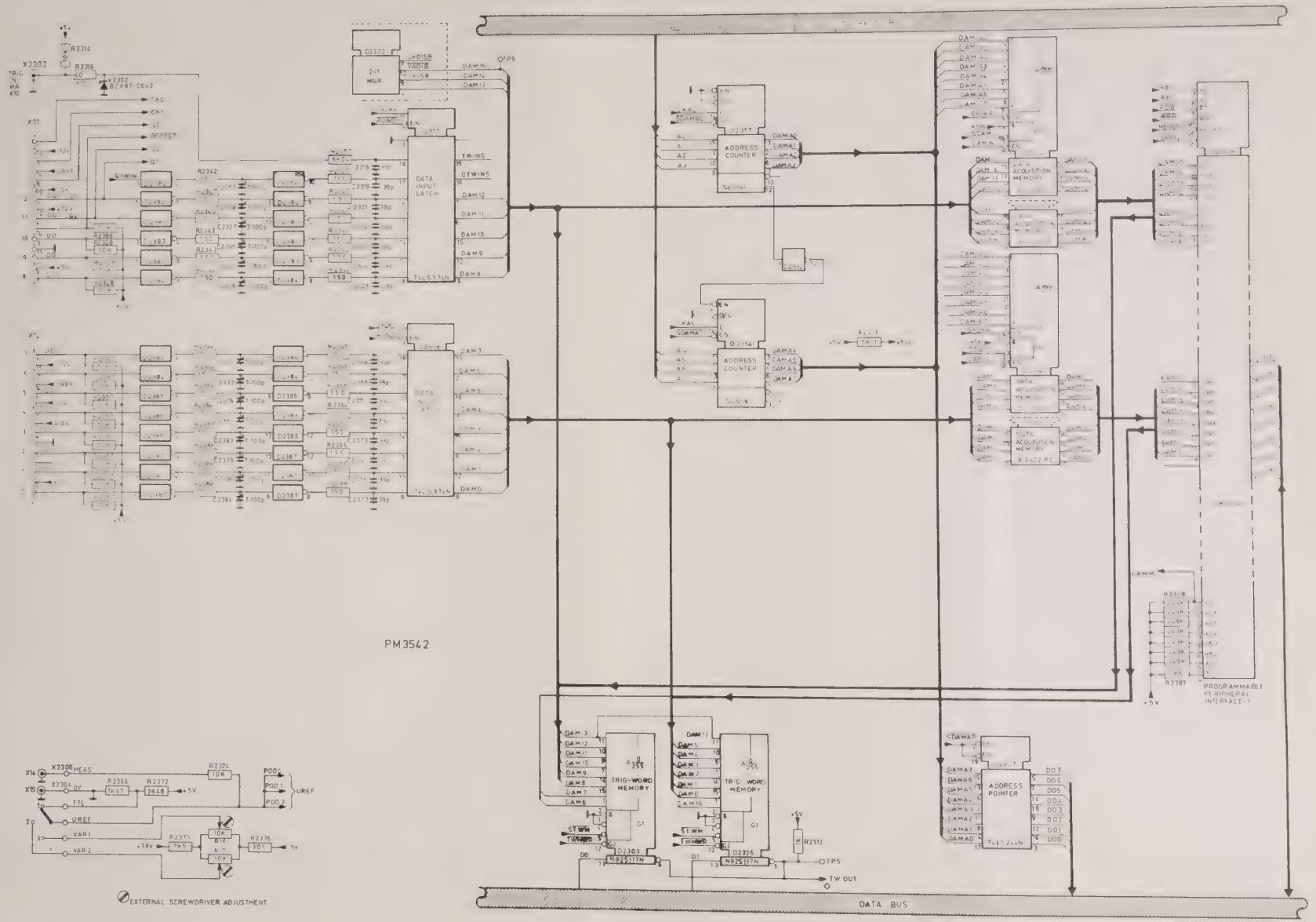

Fig. 8.1. Data acquisition circuit PM 3542

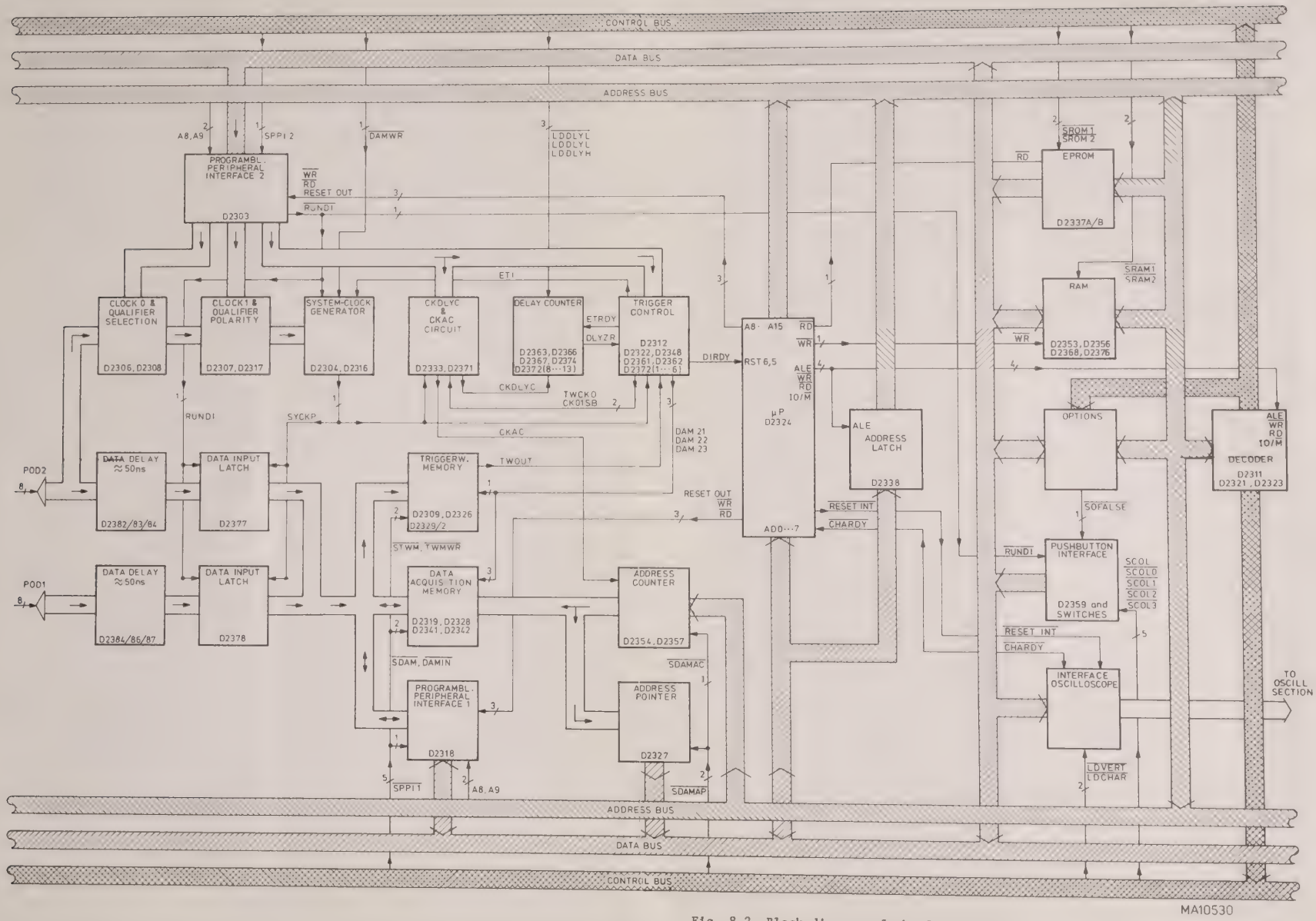

Fig. 8.2. Block diagram of the State Analyzer Part PM 3542

CODING SYSTEM OF FAILURE REPORTING FOR QUALITY ASSESSMENT OF T & M INSTRUMENTS

(excl. potentiometric recorders)

The information contents of the coded failure description is necessary for our computerized processing of quality data.

Since the reporting of repair and maintenance routines must be complete and exact, we give you an example of a correctly filled-out PHILIPS SERVICE Job sheet.

① Country	② Day Month Year	③ Typenumber /Version	④ Factory/Serial no.
3 2	1 5 0 4 7 5	0 P M 3 2 6 0 0 2	D O 0 0 7 8 3

CODED FAILURE DESCRIPTION ⑥

⑤ *Nature of call*

- [ ] Installation
- [ ] Pre sale repair
- [ ] Preventive maintenance
- [X] Corrective maintenance
- [ ] Other

Location: 0 0 2 1

Component/sequence no.

T	S	0	6	0	7
R	0	0	6	3	1
9	9	0	0	0	1

Category: 5 / 2 / 4

⑦ *Job completed*: [X]

Working time ⑧: 1 2 Hrs

Detailed description of the information to be entered in the various boxes:

①Country: 3 2 = Switzerland

②Day Month Year 1 5 0 4 7 5 = 15 April 1975

③Type number/Version O P M 3 2 6 0 0 2 = Oscilloscope PM 3260, version 02 (in later oscilloscopes this number is placed in front of the serial no)

④Factory/Serial number D O 0 0 7 8 3 = DO 783 These data are mentioned on the type plate of the instrument

⑤ Nature of call: Enter a cross in the relevant box

⑥ Coded failure description

Location

[ ][ ][ ][ ]

These four boxes are used to isolate the problem area. Write the code of the part in which the fault occurs, e.g. unit no or mechanical item no of this part (refer to 'PARTS LISTS' in the manual).

Example: 0001 for Unit 1
000A for Unit A
0075 for item 75

If units are not numbered, do not fill in the four boxes; see Example Job sheet.

Component/sequence no.

[ ][ ][ ][ ][ ][ ]

These six boxes are intended to pinpoint the faulty component.

A. Enter the component designation as used in the circuit diagram. If the designation is alfa-numeric,the letters must be written (starting from the left) in the two left-hand boxes and the figures must be written (in such a way that the last digit occupies the right-most box) in the four right-hand boxes.

B. Parts not identified in the circuit diagram:

990000 Unknown/Not applicable
990001 Cabinet or rack (text plate, emblem, grip, rail, graticule, etc.)
990002 Knob (incl. dial knob, cap, etc.)
990003 Probe (only if attached to instrument)
990004 Leads and associated plugs
990005 Holder (valve,transistor, fuse, board, etc.)
990006 Complete unit (p.w. board, h.t. unit, etc.)
990007 Accessory (only those without type number)
990008 Documentation (manual, supplement, etc.)
990009 Foreign object
990099 Miscellaneous

Category

[ ]

0 Unknown, not applicable (fault not present, intermittent or disappeared)
1 Software error
2 Readjustment
3 Electrical repair (wiring, solder joint, etc.)
4 Mechanical repair (polishing, filing, remachining, etc.)
5 Replacement (of transistor, resistor, etc.)
6 Cleaning and/or lubrication
7 Operator error
8 Missing items (on pre-sale test)
9 Environmental requirements are not met

⑦ Job completed: Enter a cross when the job has been completed.

⑧ Working time: Enter the total number of working hours spent in connection with the job (excluding travelling, waiting time, etc.), using the last box for tenths of hours.

[ ][ ][1][2] = 1,2 working hours (1 h 12 min.)

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